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# BUCK CONVERTER WITH CLOSED-LOOP VOLTAGE-MODE CONTROL

**ABDUL KADIR BIN ZAKARIA**

**Submitted to the Faculty of Electrical Engineering in partial of**
**the requirement for the award of the**
**Bachelor of Degree in Electrical Engineering**

**Faculty of Electrical Engineering**
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*Specially Dedicated to*

*My beloved Father, Mother, Brothers, Sisters and friends for their endless support, encouragement, inspiration and motivation throughout my journey of education.*

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# ABSTRACT

The main objective of the project is to provide a regulated output voltage of the buck converter using closed-loop voltage-mode control method. This project involves in designing the buck regulator circuit, simulating the circuit using PSpice software and the hardware construction of the real converter circuit. It is essential to design and simulate the circuit first before constructing the real circuit so that the expected waveform and performance of the circuit can be predicted. The softwares used in this projects are PSpice, MATLAB and Protel DXP 2004. The compensator is designed by modifying the frequency response of the open-loop buck converter circuit obtained from the simulation in PSpice. The real circuit of the power stage, controller and compensator are constructed on the (Printed circuit board) PCB and the circuits are tested to confirm the result with the theoretical predictions.

# ABSTRAK

Objektif utama projek ini adalah untuk menyediakan voltan keluaran teratur pengatur buck dengan menggunakan kaedah mod kawalan-voltan gelung tertutup untuk mengawal penukar buck. Projek ini melibatkan rekabentuk litar penukar buck serta simulasi litar menggunakan perisian PSpice. Pembinaan perkakasan litar penukar yang sebenar telah dihasilkan bagi mengesahkan hasil simulasi. Adalah penting untuk mereka dan melakukan simulasi terhadap litar terlebih dahulu sebelum membina litar sebenar untuk menjangka gelombang yang dikehendaki dan prestasi litar tersebut. Perisian yang digunakan di dalam projek ini adalah PSpice, MATLAB dan Protel DXP 2004. Pemampas direka dengan mengubah sambutan frekuensi litar penukar buck yang diperolehi daripada simulasi di dalam PSpice. Litar sebenar kuasa, pengawal dan pemampas dibina di atas (Printed circuit board) PCB dan telah diuji bagi mengesahkan keputusan teori.

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# LIST OF SYMBOLS

| | | |
|---|---|---|
| % | - | Percentage |
| PCB | - | Printed circuit board |
| V | - | Volt |
| L | - | Inductor |
| C | - | Capacitor |
| R | - | Resistor |
| D | - | Duty cycle |
| $\Delta V$ | - | Voltage Ripple |
| DC | - | Direct Current |
| $f_S$ | - | Switching Frequency |
| $i_L$ | - | Switch/Inductor Current |
| $v_{ref}$ | - | Reference Voltage |
| ESR | - | Internal Series Resistance of Capacitor |
| PS | - | Power Supply |
| $P_o$ | - | Output Power |
| CCM | - | Continuous Conduction Mode |

# CHAPTER 1

# INTRODUCTION

## 1.0 Introduction

This chapter describes the project background, objectives, scopes, and the summary of the thesis. In the project background, it briefs the description of the buck converter and the voltage-mode controller as well as the objectives and the scopes. Lastly, outline of this thesis is given in this chapter.

## 1.1 Project Background

Direct current to direct current (DC-DC) converters are power electronics circuits that converts direct current (DC) voltage input from one level to another . DC-DC converters are also known as switching converters, switching power supplies or switches. DC-DC converters are important in portable device such as cellular phones and laptops.

Why do we need DC-DC converter? For example, when we want to use a device with low voltage level, if we connected the device such as laptop or charger directly to the rectified supplied from the socket at home, the device might not functioning properly or it might be broken due to overcurrent or overvoltage. Therefore to avoid unnecessary damage to the equipments and devices, we would need to convert the voltage level to suitable voltage level for the equipments to function properly. In this project, the configuration of DC-DC converter chosen for study was buck configuration. Buck converter converts the DC supply voltage to a lower DC output voltage level. The buck converter is suitable for low power application due to the low voltage level at the output.

The control method chosen to maintain the output voltage from the buck converter was voltage-mode control. Voltage-mode control technique compares the actual output voltage with the reference voltage. The difference between both voltages will drive the control element to adjust the output voltage to a fix voltage level. This is called as voltage regulation. Voltage regulation is very important in electronic circuit to ensure the load or the connected device can operate properly and to avoid damage to the equipment from overvoltage and overcurrent.

## 1.2 Project Objectives

The main objective of this project is to design a buck converter to convert the input DC voltage to lower DC output voltage level for low power applications to solve the problem of voltage regulation and high power loss of the linear regulator circuit. The converter uses switching scheme operates the switches such as MOSFET in cut-off and saturation region to reduce power loss across the transistor or switch. The output voltage level is then regulated by the voltage-mode control circuit to a desired output voltage level as in the design specification.

## 1.3 Project Scopes

The scopes of this project are:

i. Study the operation of buck converter.

ii. Study the operation of voltage-mode control circuit.
iii. Simulation of buck converter and controller circuit using PSpice, Protel DXP 2004 and MATLAB softwares.
iv. Simulation of buck converter frequency response using PSpice software.
v. Design the buck converter power stage circuit.
vi. Design the controller and compensator circuit.
vii. Testing and calibration of the completed buck converter to confirm the actual response with the theoretical predictions.

The design specification is based on low power applications. For instance, laptop battery charger, handphone charger and etc. The circuit is simulated by using PSpice software to obtain the desired power stage response.

Table 1.1 below shows the buck regulator design specifications. Equation 1-1 is used to calculate the capacitor's internal series resistance.

$$ESR = \frac{\Delta V_O}{\Delta I_O} \tag{1-1}$$

| **Topology** | Non-isolated buck converter |
|---|---|
| **Minimum inductance ($L_{min}$)** | $93\mu H$ |
| **Frequency (f)** | 50 kHz |
| **Minimum capacitance ($C_{min}$)** | $30\mu F$ |
| **Output voltage ($V_o$)** | 7.5 V |
| **Output current ($I_o$)** | 0 to 3 A |
| **Output voltage ripple ($\Delta V_o$)** | $\pm 50mV$ |
| **Output current ripple ($\Delta I_o$)** | $\pm 0.6A$ (1%) |
| **Equivalent series resistance (ESR)** | $\frac{50mV}{0.6A} = 83m\Omega$ |
| **DC input voltage ($V_{in}$ or $V_s$)** | 9 V to 12 V, nominal = 10 V |
| **Switch selection** | IRF9540 metal-oxide-semiconductor field-effect transistor (MOSFET) |

**Table 1.1: Design specification of buck converter power stage.**

Minimum inductance is required to maintain inductor current in continuous conduction mode (CCM). Therefore, the value of selected inductance should be higher than $L_{min}$. The frequency is selected to minimize switching loss in the circuit. The output voltage is chosen based on the required voltage for handphone charger application and the value of capacitance was selected to have an output voltage ripple of $\pm 50\,\mathrm{mV}$.

Load current ($I_o$), duty cycle (D) and input voltage ($V_{in}$)values were chosen within the range that will maintain the output voltage regulated at 7.5 V. Switching device, IRF9540 MOSFET was selected for its capability of handling high switching frequency. Since the regulator is used for low power application, MOSFET is the best economical choice.

## 1.4 Outline of Thesis

This thesis consists of 6 chapters. In the first chapter, it discusses the project background, objectives, and scopes. In Chapter 2, literature reviews and theories on buck converter and switching converter are discussed.

The methodology, and equipments are discussed in Chapter 3 while the hardwares and softwares implementation are discussed in Chapter 4. In Chapter 5, results for both open-loop and closed-loop regulator are discussed. In the sixth chapter, the suggestions and conclusions obtained upon successfully completing this project is given. Finally, the last part in the thesis provides the references and appendices used in the project.

# CHAPTER 2

# THEORIES AND LITERATURE REVIEWS

## 2.0 Introduction

This chapter describes all of the related theories and literature reviews of the buck converter project.

## 2.1 Definition of Linear Voltage Regulator

Linear regulator controls the output voltage by varying the transistor base current. The output voltage is controlled between 0 V to $V_s$. The variation in input voltage or load will be compensated by adjusting the base current in order to regulate the output.

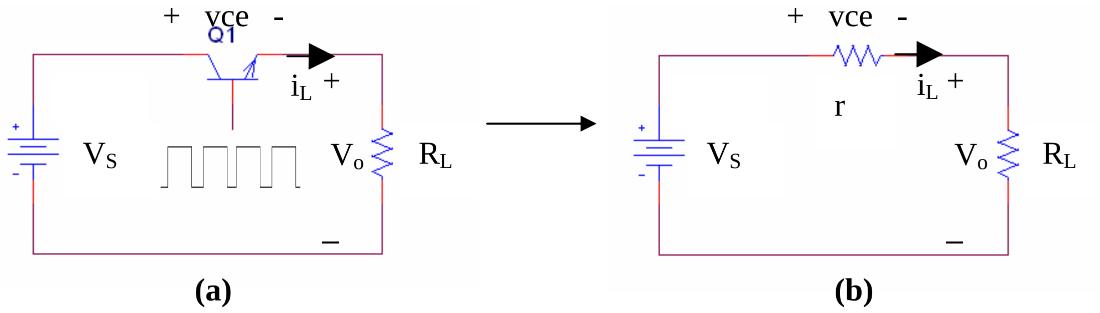
In linear regulator the transistor operates in the linear region rather than cutoff and saturation region. Effectively, the transistor acts as a variable resistance. This causes the circuit to operate with low efficiency due high power loss in the transistor. Lower output voltage results in even lower efficiency [1].

## 2.2 Linear Regulator

One method of converting a DC voltage is by using a linear voltage regulator. The voltage output is given as equation 2-1 below.

$$V_o = I_L R_L \tag{2-1}$$

If transistor is used as the control element in the regulator circuit, by adjusting the transistor base current ($i_b$), the output voltage ($V_o$), can be varied from 0 to roughly $V_s$. The base current can also be adjusted to compensate for variation in the supply voltage to regulate the output at a fixed voltage. This type of regulator is called as linear regulator since the transistor operates in a linear region. In fact, the transistor operates as variable resistance. Refer to Figure 2.1. r is the transistor equivalent resistance or variable resistor when the transistor operates in transistor linear region. Since the transistor is equivalent to variable resistance it operates in transistor linear region, thus, there is voltage drop across the transistor.



**(a)** **(b)**

**Figure 2.1: (a) Actual linear regulator circuit. (b) Linear regulator equivalent circuit**

The main drawback of a linear regulator is that the efficiency is quite low. This is due to the power loss in the transistor. The power loss in the transistor makes linear regulator inefficient. For instance, when the output is 50% of the supply voltage, thus the power loss in the transistor is 50% of the total power supplied by the source. Thus, lower output voltage result in even higher power loss and lower efficiency in the circuit.

## 2.3 Definition of DC-DC Converter

DC-DC converters are power electronics circuit that converts DC input voltage to a different DC output voltage level. It usually provides a regulated output. DC-DC converter is also known as DC-DC regulator, switching power supplies or switches and DC chopper [1].

## 2.4 Switching Converter

One way to solve the problem of linear regulator is by using a switching converter. In switching converter the transistor acts as a switch (can be turned on and off) instead of as a variable resistance. The transistor in switching converter operates in saturation and cutoff region. Assuming the switch is ideal, the output voltage is the same as the input voltage when the switch is on and zero when the switch is off. The DC component of the output voltage is calculated using equations 2-2, 2-3, and 2-4 below.

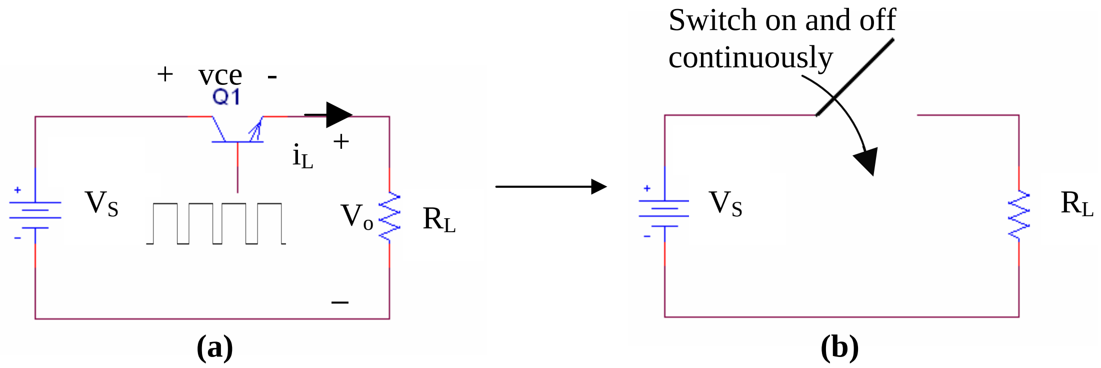
$$V_o = \frac{1}{T}\int_0^T v_o(t)dt \tag{2-2}$$

$$V_o = \frac{1}{T}\int_0^{DT} V_s(t)dt \tag{2-3}$$

$$V_o = V_s D \tag{2-4}$$

From the equation, it can be seen that the output voltage is depending on the duty ratio (D). The duty ratio is calculated as in equation 2-5 where f is the switching frequency, T is time for one complete cycle, and $t_{on}$ is the time when the switch is on.

$$D = \frac{t_{on}}{T} = t_{on} \times f \tag{2-5}$$



**(a)** **(b)**

**Figure 2.2: (a) Actual switching converter circuit. (b) Switching converter equivalent circuit.**

Figure 2.2 shows the switching converter and its equivalent circuits. When the transistor operates in cutoff and saturation region, it acts as a switch that turns on and off continuously with the period is determined by the pulse-width's duty cycle applied at the base of the transistor.

## 2.5 Definition of Buck Converter

Buck regulator is a DC-DC converter that converts higher DC voltage to lower DC voltage or step-down DC-DC converter [2].

It is also known as down converter because the output voltage is less than the input voltage [1].

## 2.6 Basic Circuit of Buck Converter

Figure 2.3 below shows the fundamental buck converter circuit with an ideal switch (S). The converter consists of a diode (D), voltage supply (Supply), inductor (L), and load (Load).

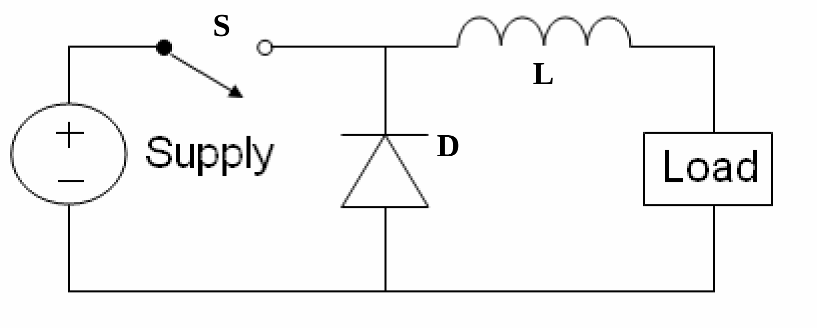


**Figure 2.3: Basic Buck Regulator Circuit**

## 2.7 Circuit Operations

An ideal buck regulator controlled the output voltage by becoming either completely on or off alternately. Figure 2.4 below will demonstrate the circuit operations when the switch is on (closed).

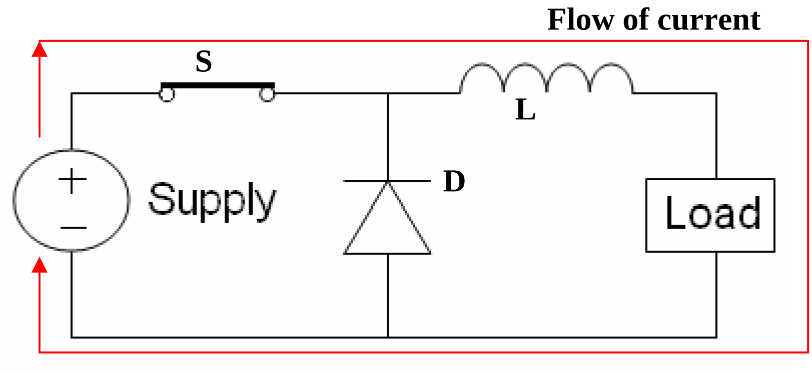


**Figure 2.4: Switch is on**

When the switch is closed (short-circuited), the current from the supply will flows through the inductor to the load and back to the supply. The arrow shows the flow of current when the switch is on. The diode is opened (reverse biased) and will not conducts.

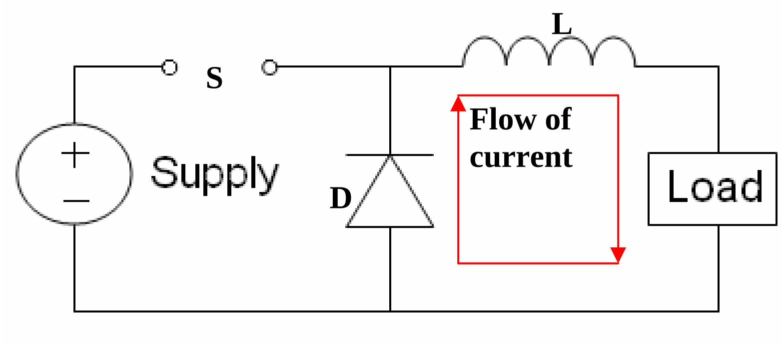


Figure 2.5: Switch is off

On the other hand, Figure 2.5 shows the flows of current when the switch is off (open). When the switch is opened (open-circuited), the energy stored in the inductor is released to the load and diode. The diode is forward biased. The arrows in the figure shows the path of current when the switch is off. The process is repeated for output voltage regulation at a fixed value. For continuous current operations, the switch will operate in on state again before the current reaches zero.

## 2.8 Power MOSFET

MOSFET is the abbreviation for metal oxide semiconductor field effect transistor. It is a very fast switching transistor that has great potential for high frequency and low power applications. Figure 2.6 below shows the IRF9540 P-channel MOSFET. The three terminals are called drain (D), source (S) and gate (G). Current flow from drain to source and the device has no reverse-blocking capability. It is a voltage-controlled majority carrier device and has positive temperature coeffiecient which means it can be cascaded to increase its current capability.[4]

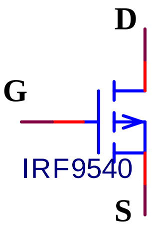


Figure 2.6: IRF9540 P-channel MOSFET

## 2.9 PSpice Software

PSpice is a software used to produce and analyze both analog and digital electronic circuits. This software is used effectively in the project to solve many problems related to voltage and current. It also capable of producing the waveforms from the analyze circuit. [5]

Figure 2.7 below is the PSpice shematic window. The menu bar consists of menu like file, edit, view and etc as shown in the figure. Menu bar helps user to search for tools to modify the schematic circuit, saving project and to simulate the project. Last added part list is a box that shows the last used component throughout the entire work process. Toolbar buttons show the icons of the options in the menu bar. It is a shortcut to the menu bar options. The scroll bars at the right side and the bottom of the window allow user to scroll the window to view the hidden part in the schematic circuit.

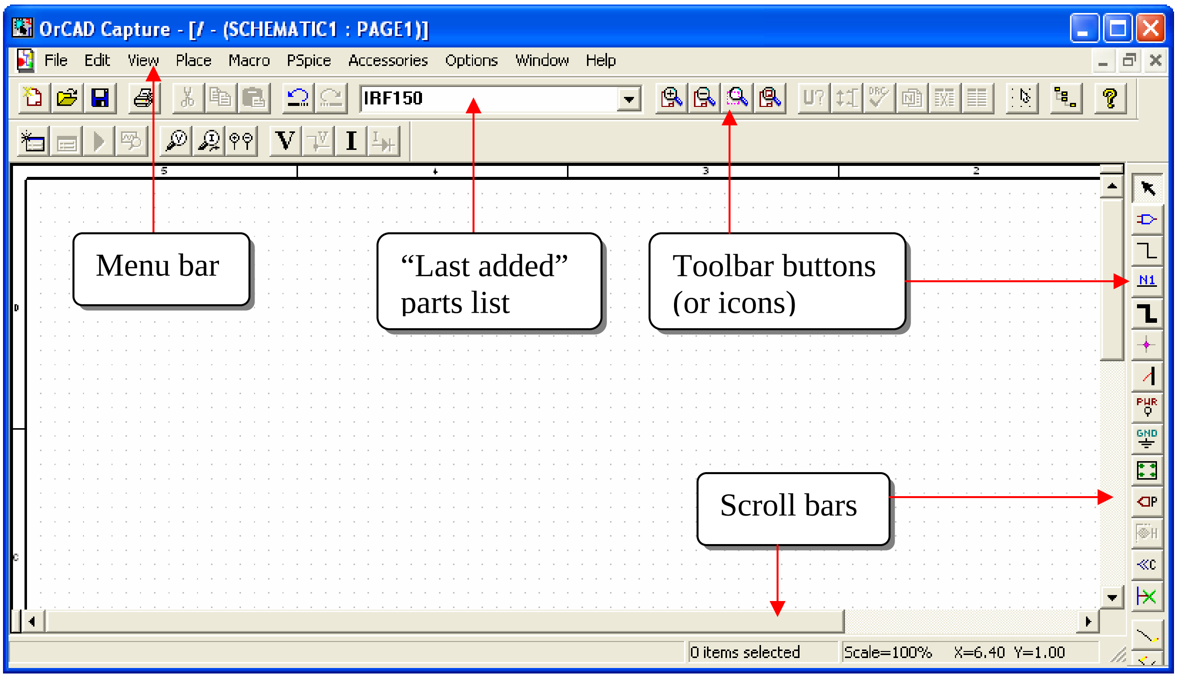
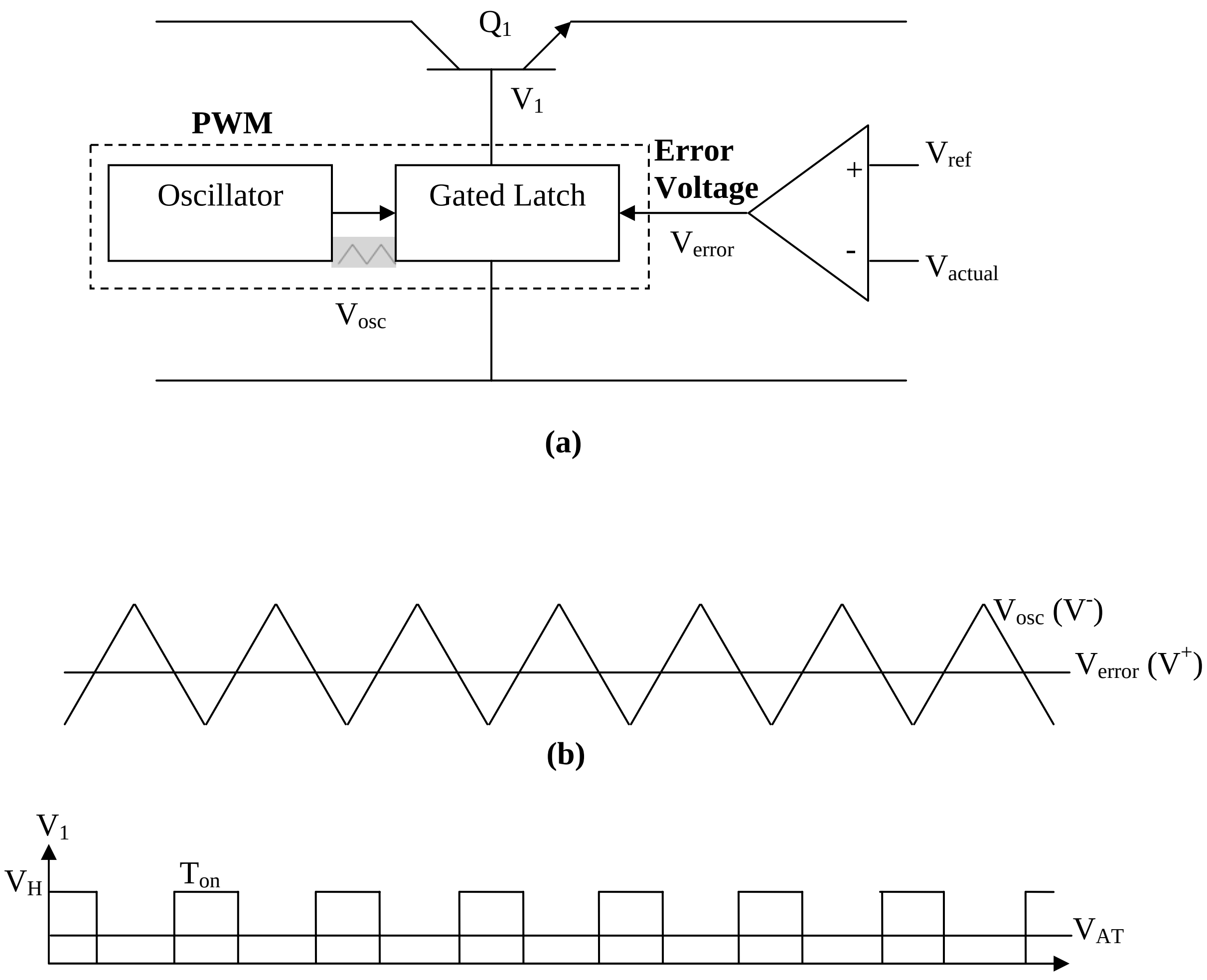


Figure 2.7 : PSpice schematic window

## 2.10 Pulse Width Modulation Circuit (PWM)

PWM circuit controls the switching rate and pulse width in buck regulator circuit. It consists of oscillator and gated latch to produce triangular waves and modulated the signal to produce series of pulse signal to the switching element.

Figure 2.8 shows a basic PWM circuit and demonstrates how series of pulse is generated from the triangular wave and control signal.



**(a)**

**(b)**

**(c)**

**Figure 2.8: (a) PWM Circuit (b) Oscillator Output, $V_{osc}$; Op-amp Output Voltage, $V_{error}$. (c) PWM Output Voltage, $V_1$**

From Figure 2.8 (b), when the control signal is larger than the triangular wave, the op-amp will generate high state and vice versa [8]. The control signal is generated by comparing the reference voltage, $V_{ref}$, with the actual voltage, $V_{actual}$, taken from the sampling circuit, to produce $V_{error}$. From the Figure 2.8 (b) also it can be seen that the pulse width is depending on the level of the error voltage. $V_H$ is the same as the peak amplitude of the triangular waveform, $T_{on}$ is the time when the duty cycle is positive and $V_{AT}$ is the average voltage of the pulse output voltage.

# CHAPTER 3

# METHODOLOGY AND EQUIPMENTS

## 3.0 Introduction

This chapter discusses on methodology and procedures as well as equipments and softwares used in the entire work process. The methodology describes how the flows of the project and procedures topic describes how the project was divided into two phase (Final year project 1 and 2) and the works involved in each phase. The work schedule topic mentioned about the used of Gantt charts for the project schedules and the equipment and software topic describes about the equipments and softwares used when the project was carried out.

## 3.1 Methodology

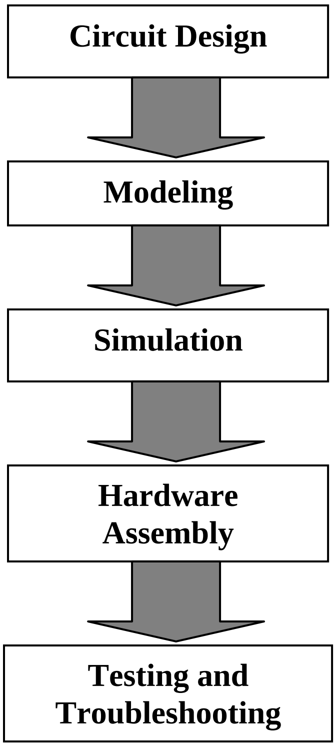


**Figure 3.1: Project methodology**

Figure 3.1 above shows that the first step in this project was to design the circuit components value for buck converter configuration. During this step, the components value were calculated using established equations and formulas.

Then models of buck converter and its controller were built and simulated using PSpice, MATLAB and Protel DXP 2004 softwares. The output and frequency response of the power stage and controller were analyzed and compared with the earlier theoretical predictions.

Next, when the simulation results had been confirmed to be approximately the same with the predictions, the power stage and controller are assembled on the PCB. The PCB circuits were built using Protel DXP 2004. The circuits were then printed on the PCB before they undergo the etching process. After the circuits had been etched properly, the hardwares of buck converter power stage and its controller on the PCB platforms were obtained. Then the components were placed and soldered on the PCBs to complete the hardwares of buck converter power stage and voltage-mode controller.

Lastly, the hardwares were tested in the lab to ensure that they function as the desired buck converter in the earlier design process. Any flaws detected on the hardwares were fixed immediately. Several numbers of tests were carried out during this step in order to make the hardwares to operate properly and accurately.

## 3.2 Procedures

The procedures involved in this project are as shown in the Figure 3.2. During final year project (FYP) 1, the works were focused on designing the buck converter power stage and the voltage-mode controller. It was started with choosing a title for the FYP 1, and ends with completed design of the converter’s power stage, first seminar and report on the FYP 1 works. In FYP 2, the works were focused on constructing the hardwares of buck converter power stage and the voltage-mode controller. It ends with final FYP 2 seminar and the submitting of completed thesis to the supervisor and the faculty. In general, the work involve in this project are shown in Figure 3.2 below.

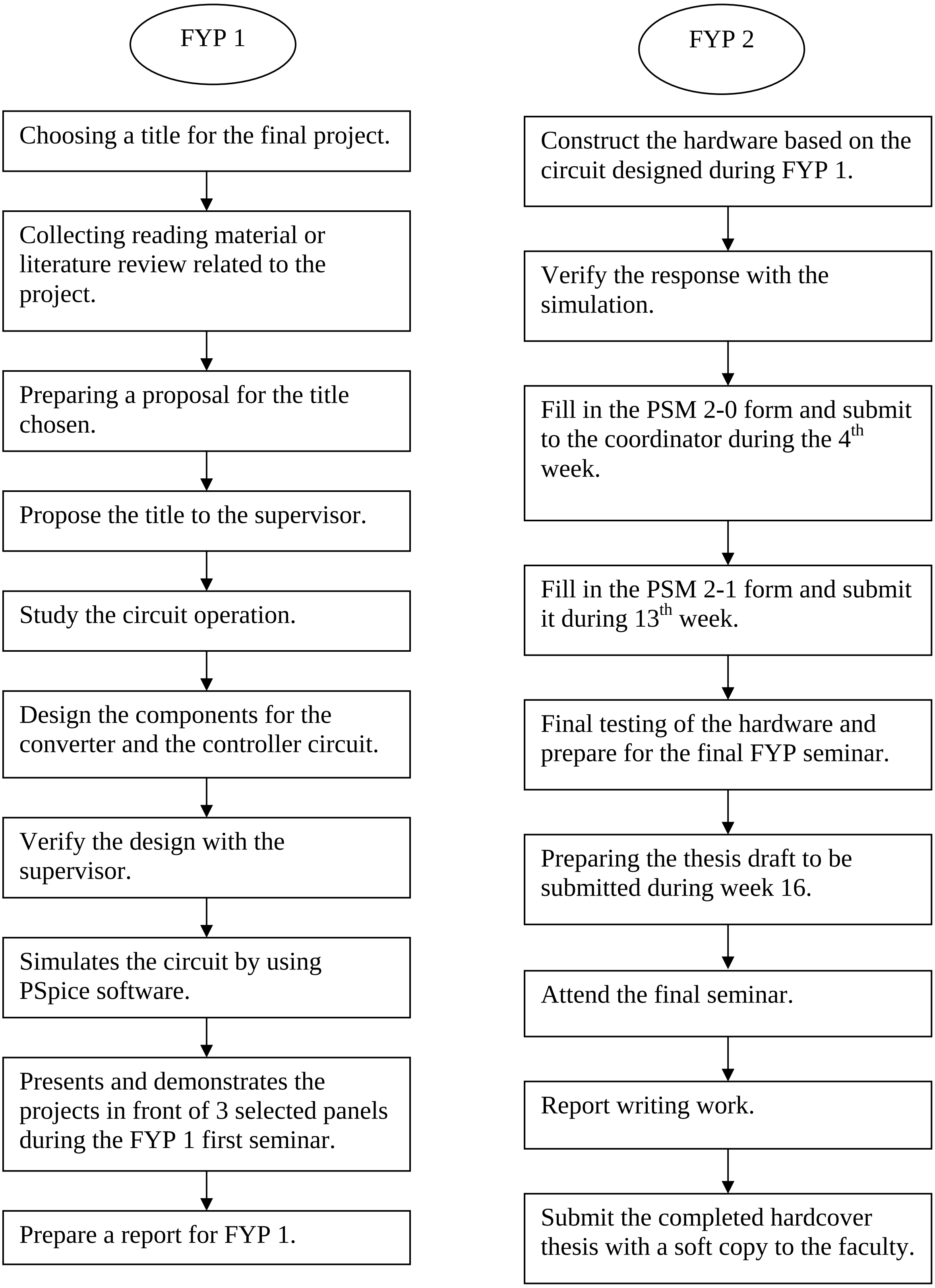


**Figure 3.2: Flow charts showing the works flow**

## 3.3 Works Schedule

Gantt chart is used to organize works schedules and to simplify the projects outline for project 1 (Appendix A) and project 2 (Appendix B). Project 1 consists of works plan on designing and simulating the buck converter and voltage-mode controller circuit using PSpice software while project 2 works plan emphasizes on constructing the hardware and thesis writing.

## 3.4 Equipment and Software

The equipment used in this project consists of hardware components and also software program to carry out the circuit simulation. The softwares used for circuit simulation were PSpice, MATLAB and Protel DXP 2004. A buck converter circuit was simulated using actual components' value to simulate the output voltage response and compared it with the desired response in the earlier design. During hardware construction phase, Protel DXP 2004 and MATLAB were used to construct the PCB circuits for buck converter power stage and its controller and to calculate the components' value for both circuits respectively.

The components used to construct the hardware of buck converter and voltage-mode controller were capacitors, resistors, inductors, diodes, MOSFET and etc. The values chosen were based on the specifications in the earlier design phase as mentioned in Chapter 1, Table 1.1.

# CHAPTER 4

# HARDWARE DESIGN AND SIMULATION

## 4.0 Introduction

This chapter describes about the hardware design and how the circuit of buck converter power stage and voltage-mode controller were simulated using PSpice, MATLAB and Protel DXP 2004 softwares.

## 4.1 Power Stage Design

The components for power stage of buck converter were calculated using equation 4-1 through equation 4-8 as shown below. $V_{sat}$ is the power-switch conduction voltage drop (assume $V_{sat}$ = 0.5 V), $V_d$ is the diode voltage drop (assumed $V_d$ = 0.6 V), and $V_{in}$ is ranging between 9 to 12 V.

$$\Delta I_o = 2 \times \text{current regulation } \times I_{o(\max)} \tag{4-1}$$

$$L_{\min} = \frac{(1-D)R_L}{2 f_s} \tag{4-2}$$

$$L_{\min} = \frac{(1-D)R_{\max}}{2 f} \tag{4-3}$$

$$C_{\min} = \frac{(1-D)V_o}{\Delta V_o \times 8Lf_s^{\ 2}} \tag{4-4}$$

$$C_{\min} = \frac{(1-D)V_o}{8L_{\min} f^{2} \Delta V_o} \tag{4-5}$$

$$V_L = V_{in} - V_{sat} - V_o \tag{4-6}$$

$$D = \frac{V_o}{V_s} \tag{4-7}$$

$$D = \frac{V_o + V_d}{Vi - V_{sat}} \tag{4-8}$$

The results obtained from the calculations were as shown in the Table 4.1 below.

| **Parameter** | **Equation** | **Chosen Value** |
|---|---|---|
| **$\Delta$ I$_o$** | $\Delta I_o = 3 \times 2 \times 0.1 = 0.6A$ | 0.6 A |
| **L$_{\min}$** | $L_{\min} = \frac{V_L D}{\Delta I_o \times f_s} = \frac{(12-0.5-7.5)\times 0.7}{0.6 \times 50k} = 93\mu H$ | $220\mu H$ |
| **C$_{\min}$** | $C_{\min} = \frac{\Delta I_o}{8 f_s \times \Delta V_o} = \frac{0.6}{8 \times 50k \times 0.05} = 30\mu F$ | $1000\mu F$ |
| **D** | $V_{in} = 12V, V_o = 7.5V$<br>$D = \frac{V_o + V_d}{Vi - V_{sat}} = 0.7$ | 0.7 |

**Table 4.1: Buck converter power stage components value**

From the calculation, the minimum value for inductance and capacitance are 93 uH and 30 uF respectively. The inductor and capacitor value is chosen to be higher than the minimum value to maintain continuous-current mode operation with 1% ripple and to limit the ripple in the output voltage waveform at 0.05 V. The chosen value of inductor and capacitor used in the project are 220 uH and of 1000 uF respectively.

### 4.1.1 Power Stage Simulation

The buck converter power stage in Figure 4.1 is simulated using PSpice software to obtain the output voltage and current response. The pulse-width generator equivalent generates the pulse-width modulation to control the P-channel MOSFET to either on or off. TF is the time for the pulse to fall to zero and TR is the time for the pulse to rise positive 12 V value. PW is the time for positive pulse-width, PER is the period for 1 complete cycle, Duty_cycle is the positive duty cycle and Switching_freq is the desired switching frequency for the MOSFET. The components value of the power stage is selected to be the same with the selected values in Table 4.1. Load is selected to be 15 ohm and the input voltage is set to 12 V. The current probe and voltage probe is used to measure the voltage and current at the inductor and the load respectively. Figure 4.2 shows the circuit built in Protel DXP 2004. The circuit was printed on the printed circuit board (PCB) before it underwent the etching process.

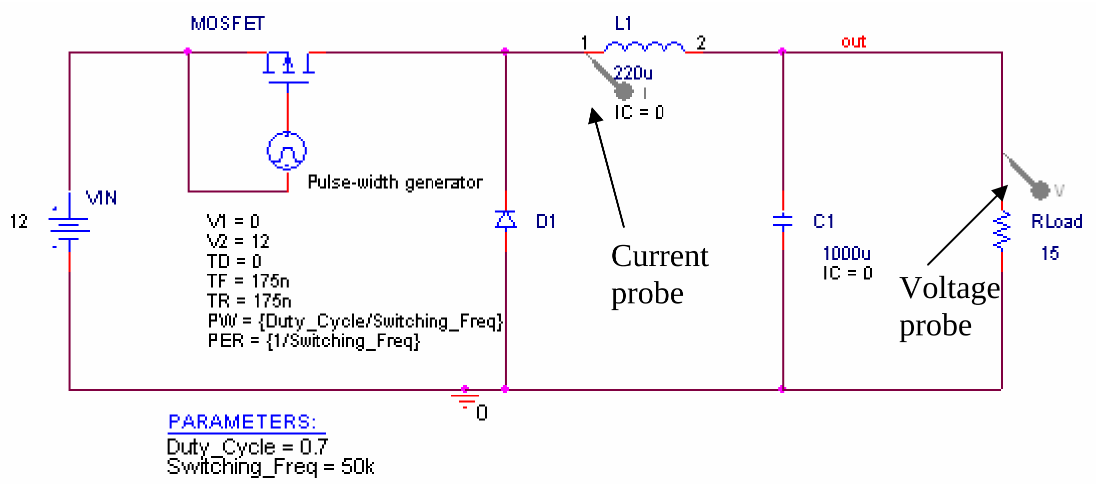


**Figure 4.1: Simulation of buck converter's power stage in PSpice**

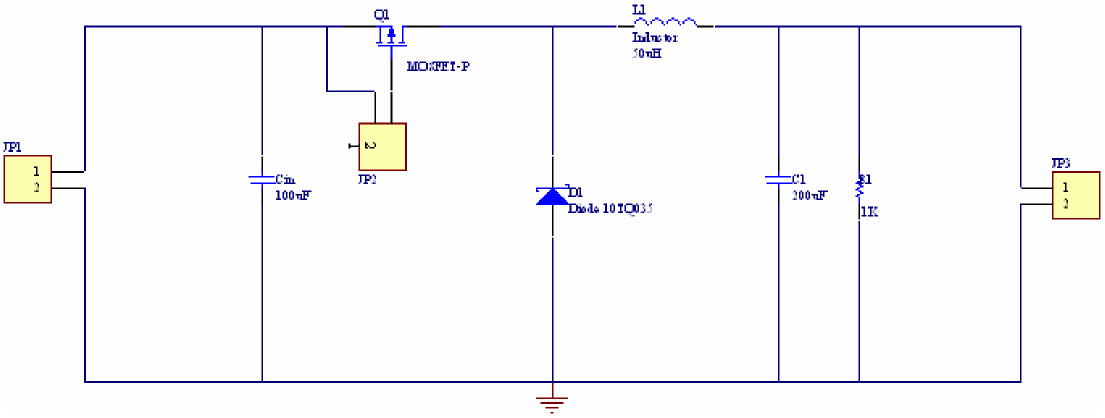


Figure 4.2: Buck converter's power stage built in Protel DXP 2004

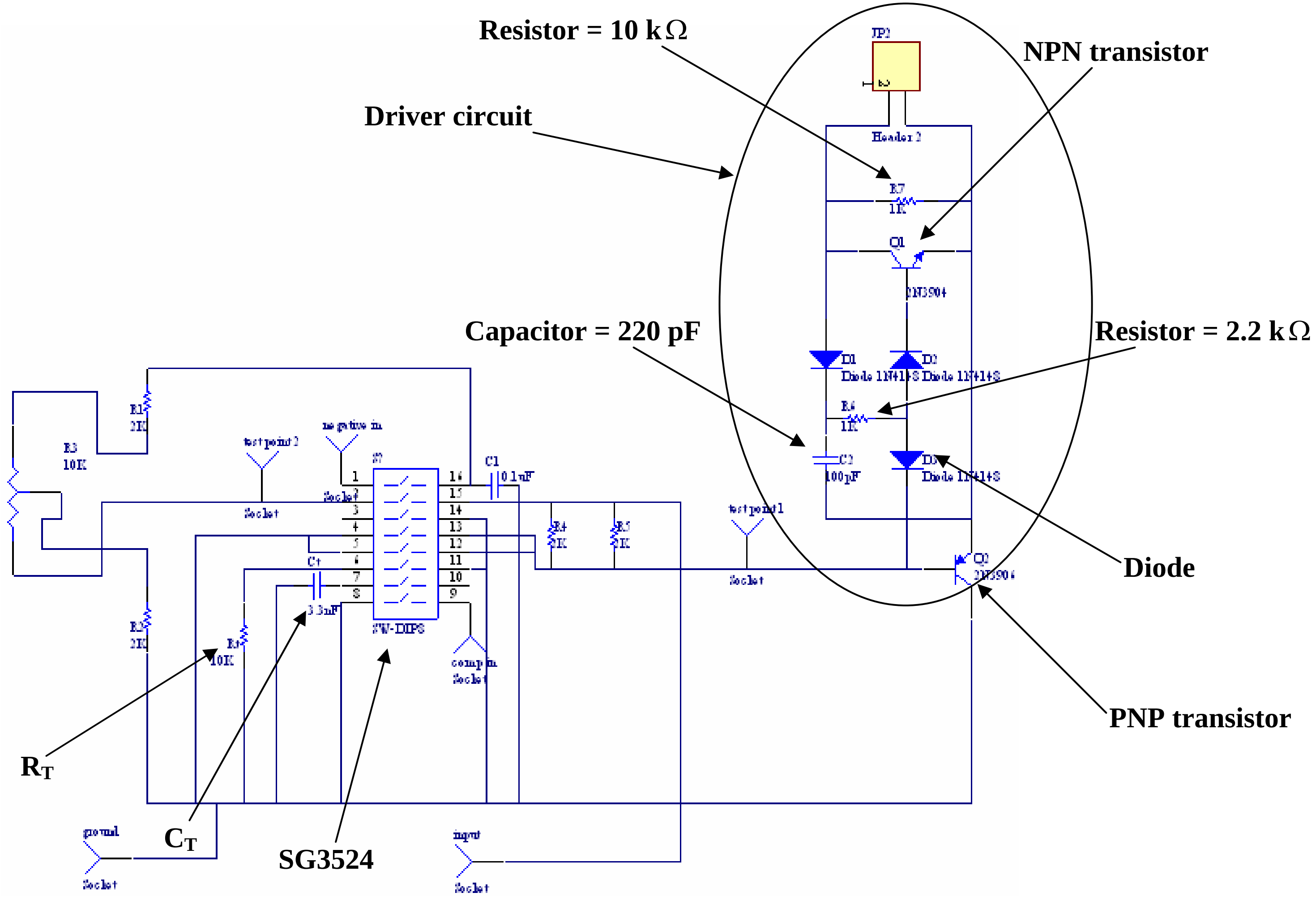
### 4.1.2 Power Stage Transfer Function

Equation 4-9 shows the transfer function of the buck converter power stage obtained from International Rectifier's application note [9]. $R_c$ is the ESR of the capacitor, L and C is the selected value as in Table 4.1.

$$\text{Power Stage} = \frac{sV_sR_c + V_s}{LCs^2 + s(\frac{L}{R} + R_cC) + 1} \tag{4-9}$$

## 4.2 Controller Design

Figure 4.3 shown below is the controller and driver circuit of the buck converter constructed in Protel DXP 2004. Integrated circuit (IC) SG3524 was used to generate series of pulse-width to trigger the MOSFET on and off.


Resistor = 10 kΩ

NPN transistor

Driver circuit

Capacitor = 220 pF

Resistor = 2.2 kΩ

Diode

PNP transistor

$R_T$

$C_T$

SG3524

Figure 4.3: Controller and driver circuit built in Protel DXP 2004

The IC SG3524 was represented by SW-DIP8 components in Protel DXP 2004. The driver circuit was built to drive the P-channel MOSFET. It consists of one NPN transistor (2N2222A), one PNP transistor (2N2907), one 10 kΩ resistor, one 2.2 kΩ resistor, one 220 pF capacitor and 3 diodes (1N4148). The controller circuit is similar to SG3524 test circuit as shown in Appendix C.

### 4.2.1 Frequency Selection

The switching frequency is selected to be 50 kHz. The frequency was selected to be less than 100 kHz since the switching loss at 50 kHz is smaller compared to switching loss at frequency of 100 kHz. In the controller circuit, the switching frequency is determined by $R_T$ and $C_T$ values as shown in Figure 4.3. Equation 4-10 was used to calculate the value for $R_T$ and $C_T$ for 50 kHz switching frequency.

$$frequency = \frac{1.3}{R_T C_T} \tag{4-10}$$

For $C_T$ = 6.8 nF, the $R_T$ is chosen to be 3800 ohm. The reference voltage is adjusted to 2.5 V and the driver circuit is constructed to drive P-channel mosfet.

### 4.2.2 Controller Transfer Function

Equation 4-11 is the transfer function of the controller and the driver circuit [1]. $V_{triangular}$ is the maximum voltage of the triangular waveform generated by IC SG3524.

$$\text{Controller} = \frac{1}{V_{triangular}} \tag{4-11}$$

## 4.3 Compensator Design

### 4.3.1 Compensator Transfer Function

The compensator transfer function is shown in equation 4-12 [10]. The values of R4, R5, R6, R7, C1, C2, and C3 were obtained from equations which are discussed in the next topics.

Compensator =

$$\left(\frac{1}{sR_5(C_1+C_2)}\right)\left(\frac{s(R_5+R_7)C_3+1}{sR_7C_3+1}\right)\left(\frac{sR_4C_2+1}{sR_4\left(\frac{C_1C_2}{C_1+C_2}\right)+1}\right) \tag{4-12}$$

### 4.3.2 Output Sense Network

Output sense network is a resistive voltage divider used to sense the changes in output voltage at the converter output. The components value for the divider circuit must be chosen carefully to maintain accuracy as high as possible. The worst-case SG3524 input bias current is 2 uA (see Appendix C). The divider current is chosen to be 1000 times greater than the worst-case value.

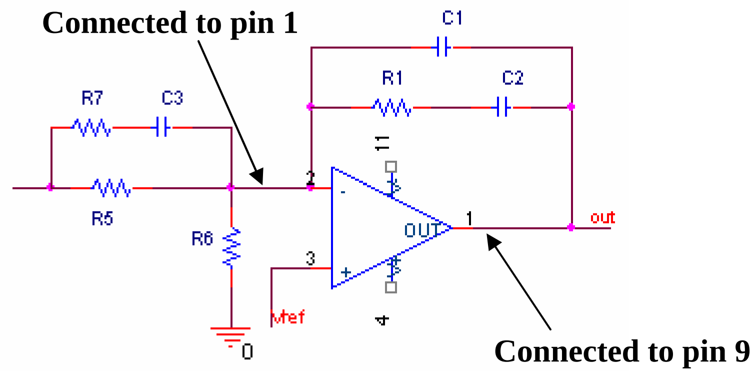
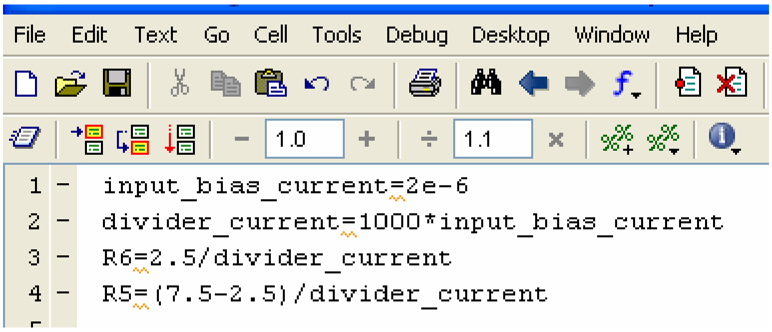


**Figure 4.4: Compensator**

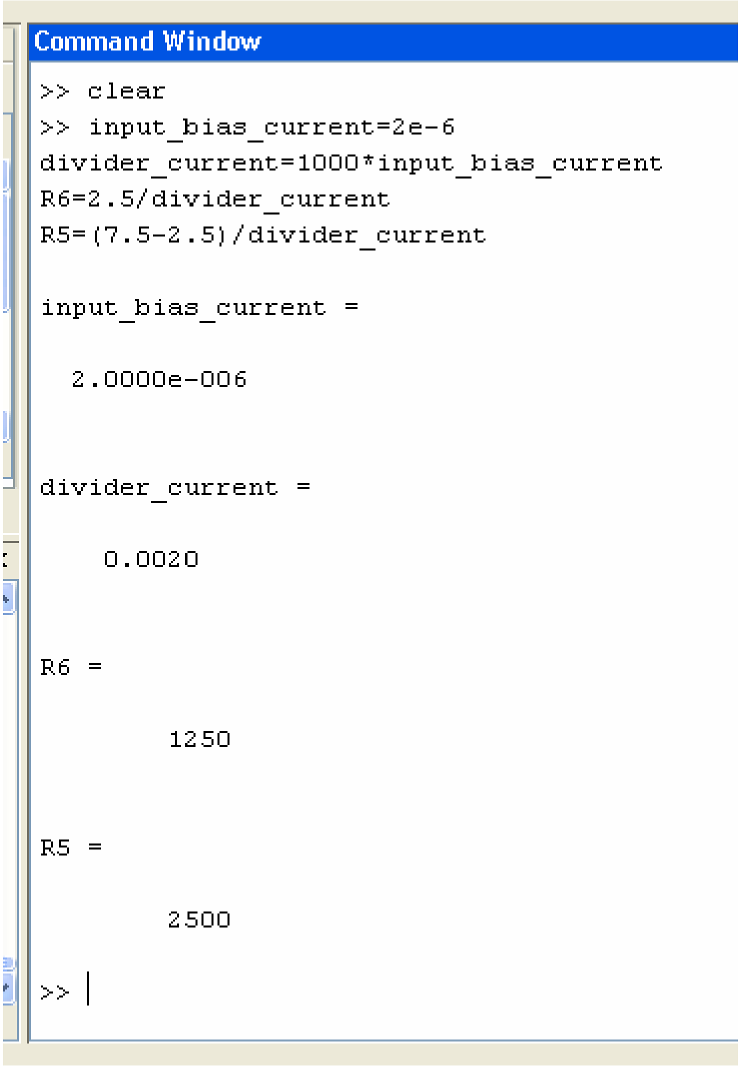
The value of resistors in the divider network are calculated using MATLAB. Figure 4.5 shows the program used in MATLAB to calculate the resistors' value.



```
input_bias_current=2e-6
divider_current=1000*input_bias_current
R6=2.5/divider_current
R5=(7.5-2.5)/divider_current
```

**Figure 4.5: MATLAB programming to calculate the resistive divider components**

Figure 4.6 shows the results of the simulation in MATLAB software to calculate the value of R5 and R6.



```
>> clear
>> input_bias_current=2e-6
divider_current=1000*input_bias_current
R6=2.5/divider_current
R5=(7.5-2.5)/divider_current

input_bias_current =

  2.0000e-006


divider_current =

    0.0020


R6 =

        1250


R5 =

        2500

>> 
```

**Figure 4.6: Results of R5 and R6 calculation in command window.**

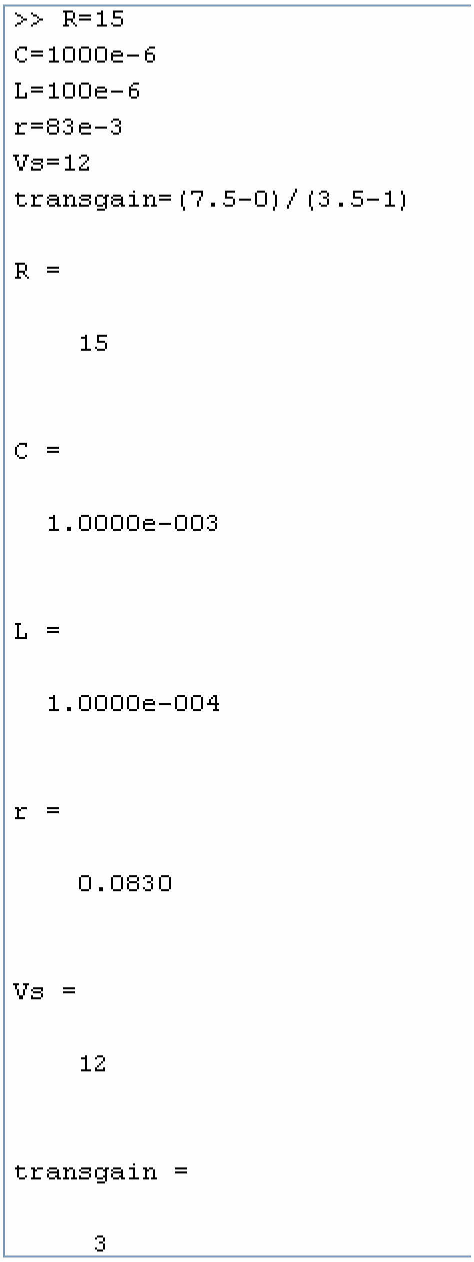
### 4.3.3 Loop Compensation Design

The loop compensator was designed to reshaping the error-amplifier/controller frequency response with external components to stabilize the DC-DC converter.

The gain of the controller circuit is calculated using the equation 4- 13.

$$A_{PWM} = \frac{\Delta V_o}{\Delta V_o (COMP)} \tag{4-13}$$

The gain was calculated using MATLAB. Figure 4.7 is the simulation result from command window.



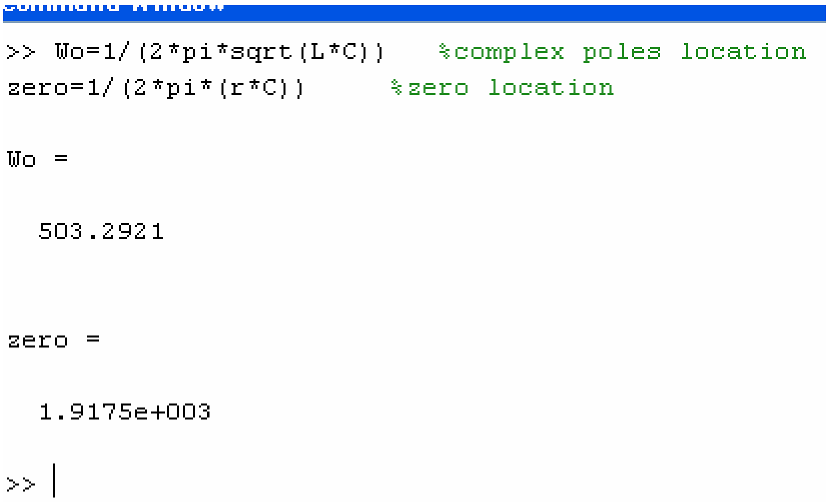
```
>> R=15
C=1000e-6
L=100e-6
r=83e-3
Vs=12
transgain=(7.5-0)/(3.5-1)

R =

    15


C =

  1.0000e-003


L =

  1.0000e-004


r =

    0.0830


Vs =

    12


transgain =

     3
```

**Figure 4.7: MATLAB simulation result of gain calculation.**

The output filter is an LC filter and function accordingly. The inductor and capcitor produces two underdamped complex-pole pair at the filter resonant frequency which is at frequency of 503.2921 Hz and the ESR puts a zero in the response above the resonant frequency which is at frequency of 1.9175 kHz. The complex poles and zeros are determined using MATLAB. The simulation results are shown in Figure 4.8 below.

$$\text{Complex poles location} = \omega_o = \frac{1}{2\pi\sqrt{LC}} \tag{4-14}$$

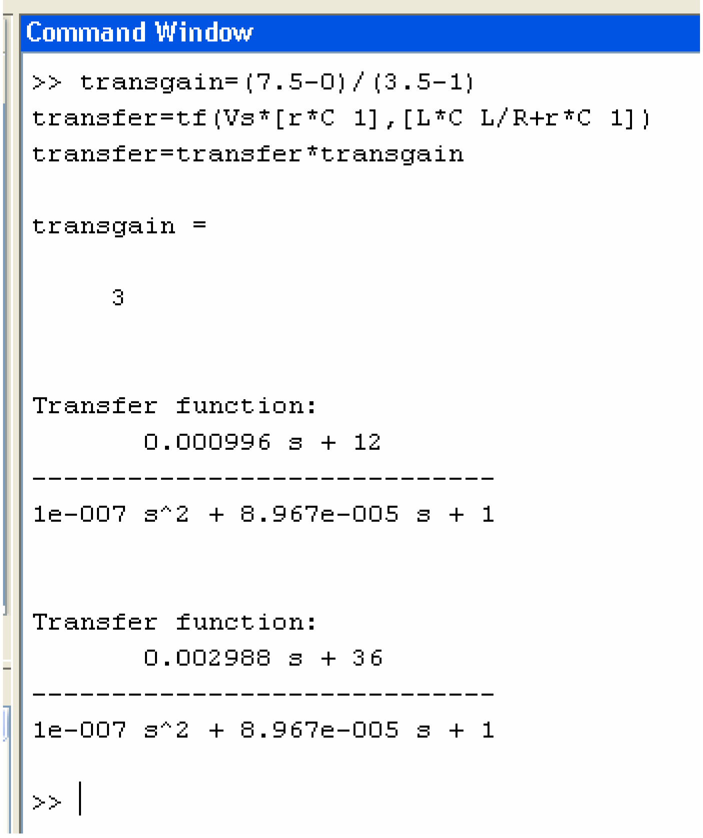
$$\text{Zero location} = \frac{1}{2\pi R_c C} \tag{4-15}$$



```
>> Wo=1/(2*pi*sqrt(L*C))    %complex poles location
zero=1/(2*pi*(r*C))      %zero location

Wo =

  503.2921


zero =

  1.9175e+003

>> |
```

**Figure 4.8: MATLAB simulation result for the location of complex poles and zero.**

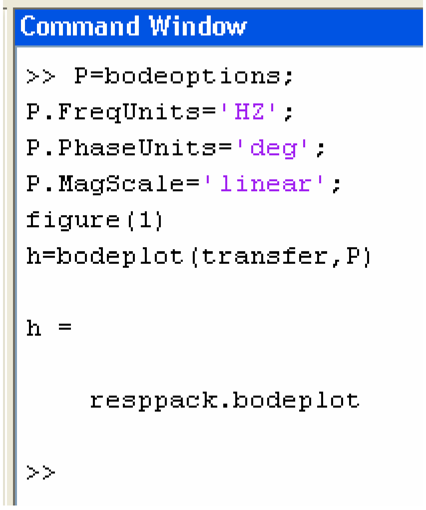
The the gain and phase plots for open-loop buck converter are obtained by multiplying the controller gain with the power stage transfer function. The simulation is shown in Figure 4.9.



```
>> transgain=(7.5-0)/(3.5-1)
transfer=tf(Vs*[r*C 1],[L*C L/R+r*C 1])
transfer=transfer*transgain

transgain =

     3


Transfer function:
       0.000996 s + 12
------------------------------
1e-007 s^2 + 8.967e-005 s + 1


Transfer function:
       0.002988 s + 36
------------------------------
1e-007 s^2 + 8.967e-005 s + 1

>> |
```

**Figure 4.9: Open-loop buck converter transfer function from command window .**

The results of simulation of open-loop buck converter and the frequency response graphs are shown in Figure 4-10 and Figure 4.11.



```
>> P=bodeoptions;
P.FreqUnits='HZ';
P.PhaseUnits='deg';
P.MagScale='linear';
figure(1)
h=bodeplot(transfer,P)

h =

    resppack.bodeplot

>>
```

**Figure 4.10: The result of MATLAB simulation of buck converter frequency response in command window.**

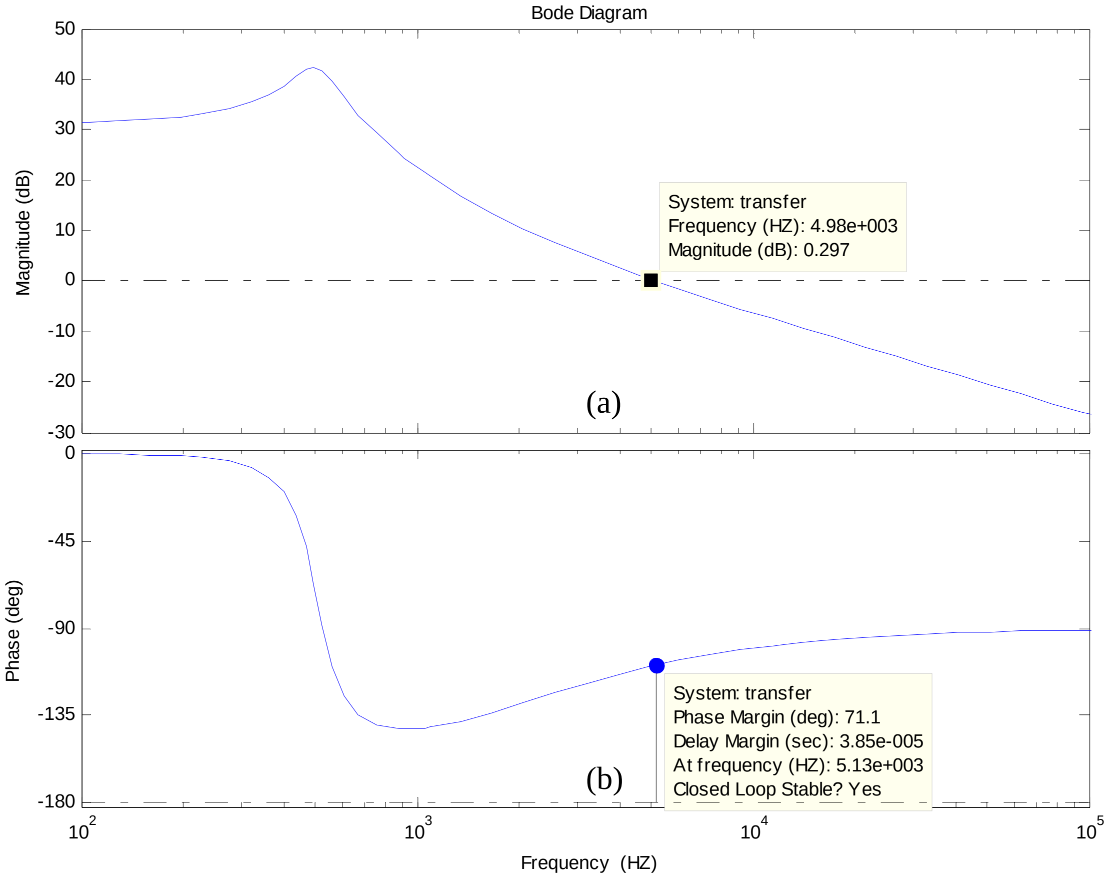


**Figure 4.11: (a) Gain response of open-loop buck converter. (b) Phase response of open-loop buck converter.**

The integrator gain (Refer to Figure 4.4), 1 / (sR5 x (C2 + C1)), establishes the open-loop unity-gain frequency. The zero will be located at approximately the same frequency as the output-filter poles to compensate for gain reduction and phase shift. The compensation network will have two zeros at f = 500 Hz to cancel out the complex poles from the LC filter. They contribute a gain of 40 dB at f = 5 kHz. From the magnitude response graph, at f = 5 kHz, the gain is 0.266 dB. Thus, the gain contributed by the compensation network's integrator should be 0 – (0.297+40) = -40.27 dB = 0.009.

The pole at $1/(2\pi R_7 C_3)$ is positioned at approximately the same frequency as the zero above the filter resonant frequency to maintain 20 dB/decade roll-off in the gain response.

The final pole at $1/(2\pi R_4 C_1 C_2 /(C_1 + C_2))$ is placed at f = 37.5 kHz to minimize high-frequency noise at the pulse-width modulator.

The components for the compensator design are calculated using MATLAB. The formulas, programming and the simulation results are as shown below.

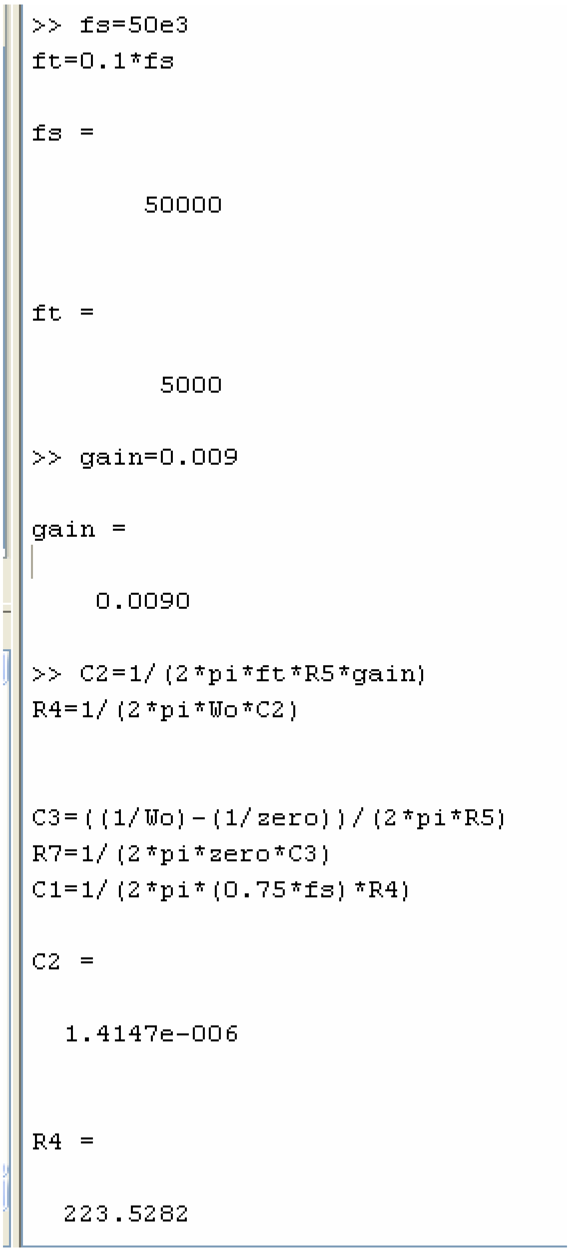
$$C2 = \frac{1}{2\pi f_t R5 \times gain} \tag{4-16}$$

$$R4 = \frac{1}{2\pi \omega_o C2} \tag{4-17}$$

$$C3 = \frac{(\frac{1}{\omega_o} - \frac{1}{zero})}{2\pi \times zero \times C3} \tag{4-18}$$

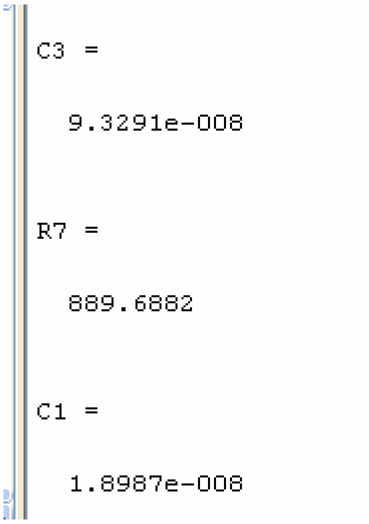
$$R7 = \frac{1}{2\pi \times zero \times C3} \tag{4-19}$$

$$C1 = \frac{1}{2\pi (0.75 \times f_s) R4} \tag{4-20}$$



```
>> fs=50e3
ft=0.1*fs

fs =

       50000


ft =

        5000

>> gain=0.009

gain =

    0.0090

>> C2=1/(2*pi*ft*R5*gain)
R4=1/(2*pi*Wo*C2)


C3=((1/Wo)-(1/zero))/(2*pi*R5)
R7=1/(2*pi*zero*C3)
C1=1/(2*pi*(0.75*fs)*R4)

C2 =

  1.4147e-006


R4 =

  223.5282
```

Figure 4.12: MATLAB simulation for compensator design (part 1)



```
C3 =

  9.3291e-008


R7 =

  889.6882


C1 =

  1.8987e-008
```

**Figure 4.13: MATLAB simulation for compensator design (part 2)**

The actual value of the components above are chosen according to its availability in the market. Thus, the components used for the compensator are R5 = 2500 ohm (2400 ohm), R6 = 1250 ohm (1200 om), C2 = 1.4147 uF (1 uF), R4 = 223.5282 ohm (240 ohm), C3 = 93.29 nF (0.082 uF), R7 = 890 ohm (910 ohm), and C1 = 18.99 nF (0.015 uF).

### 4.3.4 Closed-Loop Buck Converter Frequency Response

Figure 4.14 and Figure 4.15 are the circuit and waveforms obtain from simple PSpice simulation.

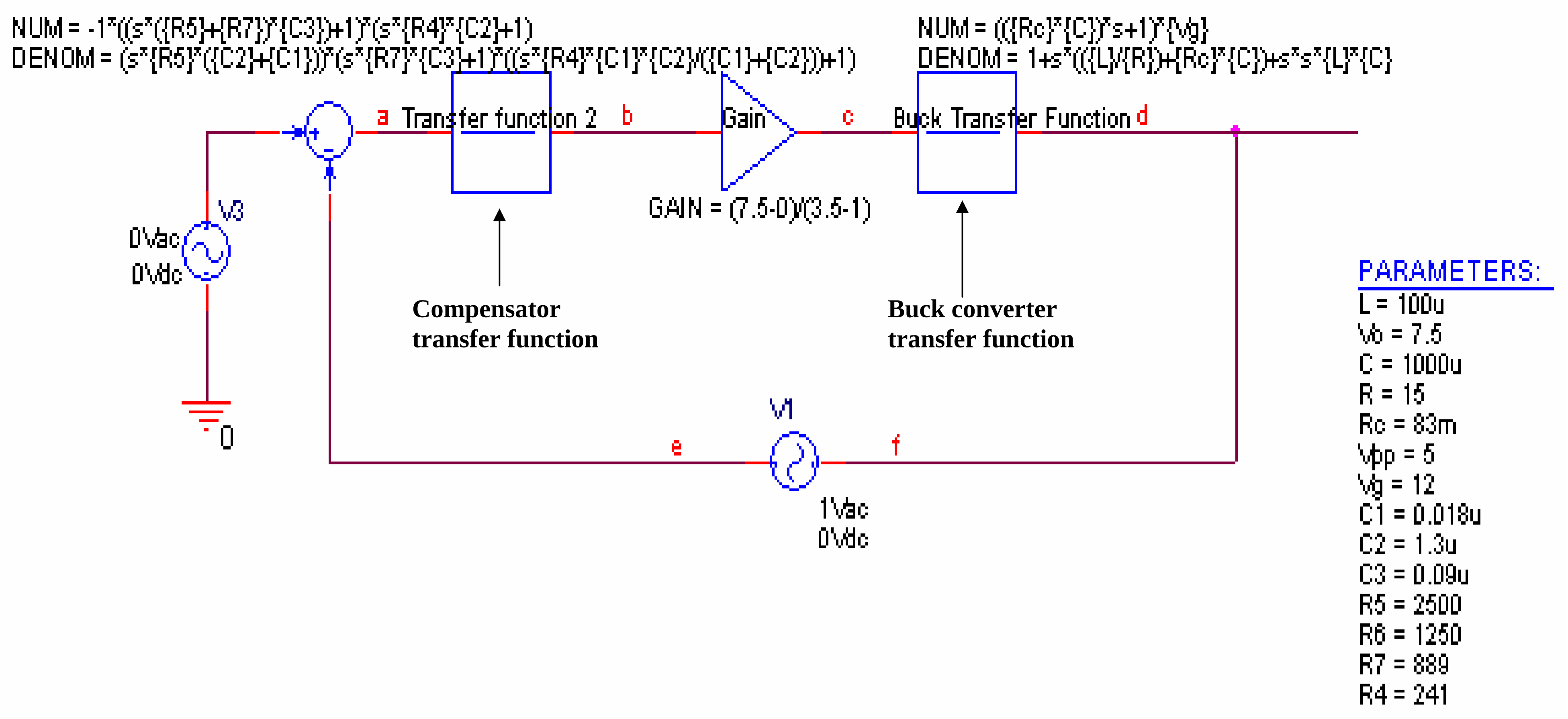
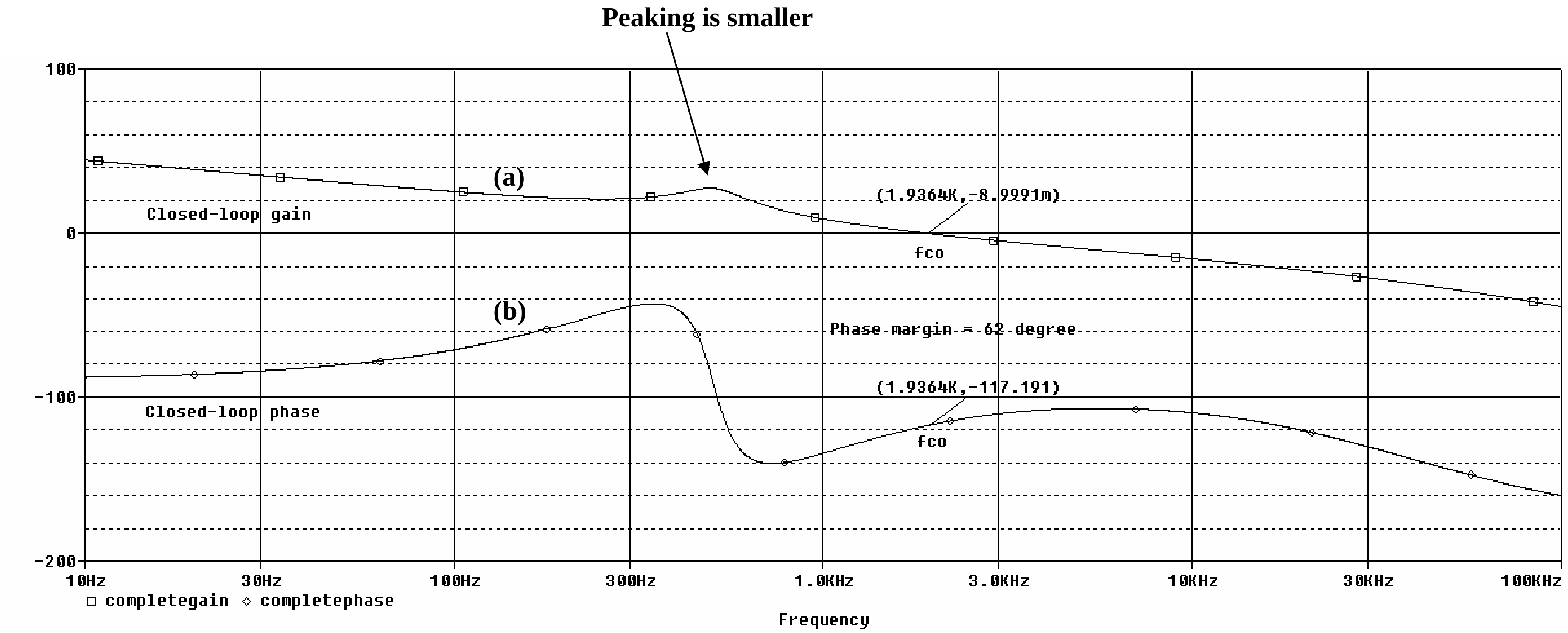


Figure 4.14: Circuit to simulate closed-loop buck converter frequency response



**Peaking is smaller**

Figure 4.15: Closed-loop buck converter frequency response (a) Gain response (b) Phase response

From the frequency response analysis, after the compensator is added to the controller, the overall response of the open-loop buck converter had been improved. From the graph, it could be seen that the peaking due to complex pole pair had been reduced and the phase margin value is equal to 62 degree.

# CHAPTER 5

# RESULTS

## 5.1 Initial Results

Buck converter circuit is build using PSpice to simulate the output voltage response. The components value used in the simulation are the actual values available in the market. The circuits and output responses are as shown below.

### 5.1.1 Simulation Results

#### 5.1.1.1 Practical Buck Regulator

Figure 5.1 shows the practical buck converter simulation using PSpice software. The values for inductor and capacitor were chosen to be the same as in Table 4.1.

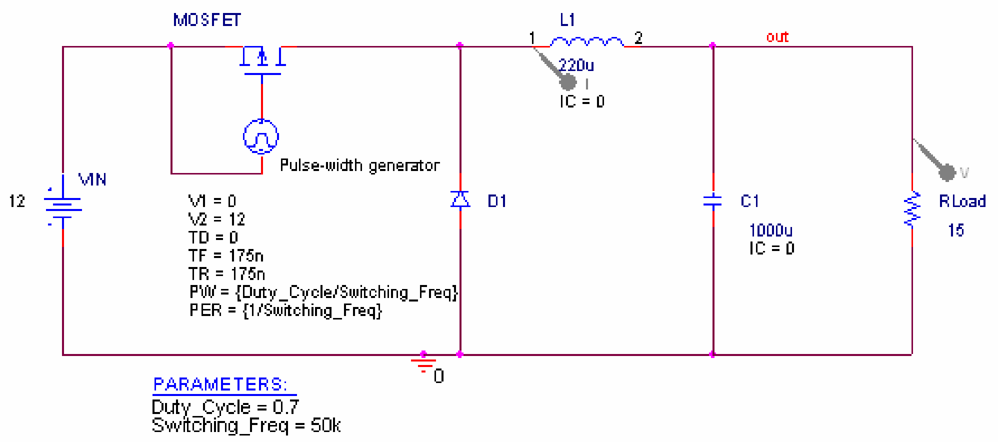


Figure 5.1: Buck converter schematic

### 5.1.1.2 Output Response

Figure 5.2 shows the output voltage and current waveforms measured at the load and inductor respectively. The voltage waveform shows that the waveform reaches 9 V peak at t = 1 ms. The voltage stabilizes at 7.5 V after approximately 8 ms.

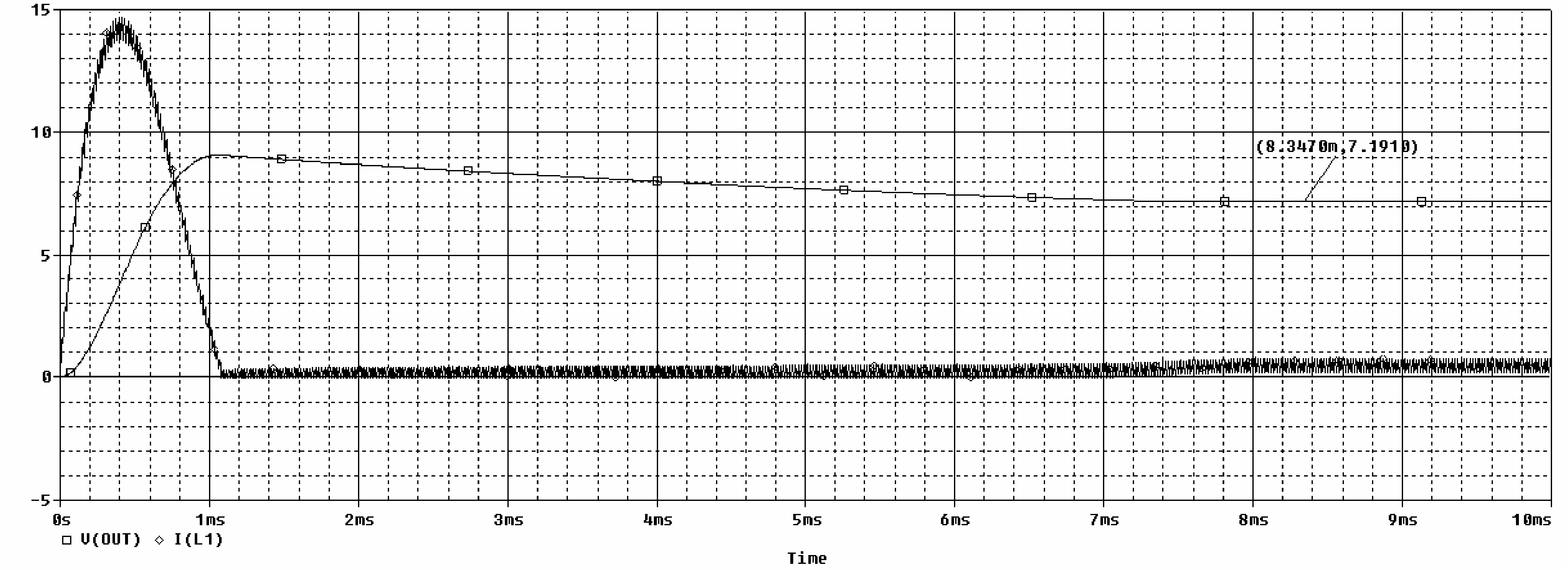


Figure 5.2: The output voltage and inductor current waveform

Figure 5.3 shows the output voltage waveform after waveform is zoomed in. From the figure, it can be seen that the voltage ripple is approximately 8.604 m – 8.595 m = 9 uV. This value is even lower than the design value for output voltage ripple which is 50 mV. Thus, from the simulation, this value had met the design requirement for output voltage ripple in the buck converter design.

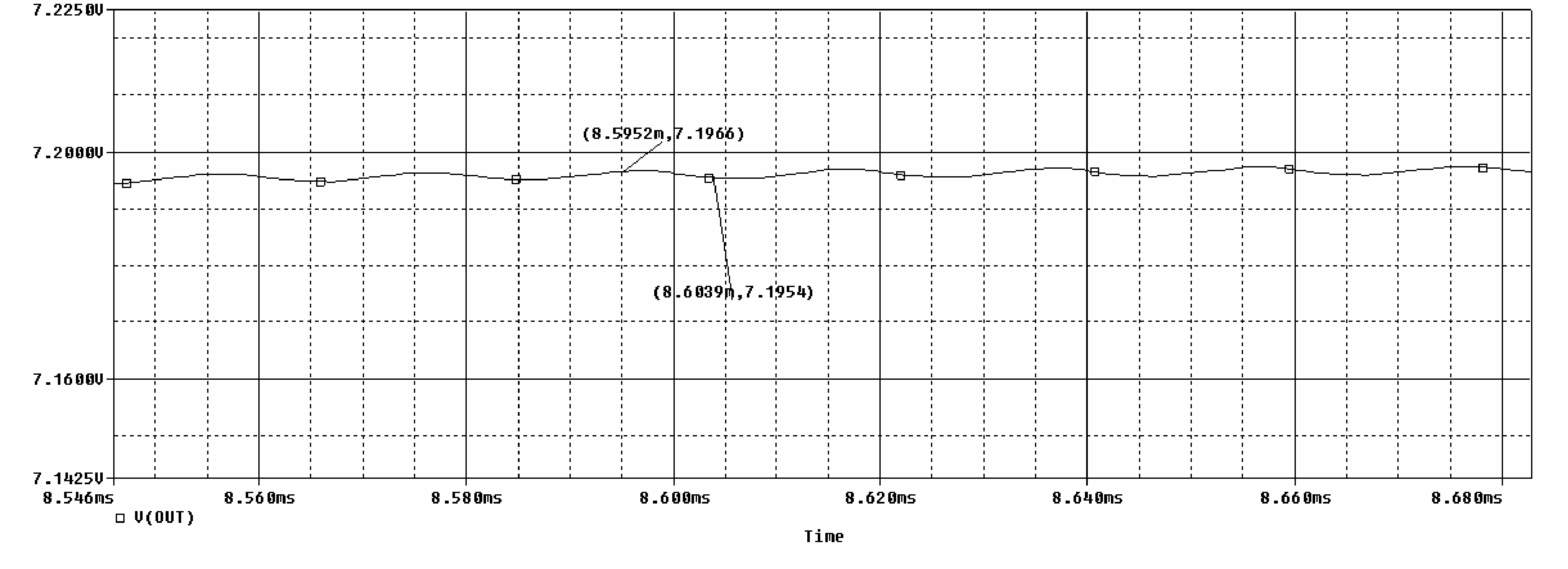


Figure 5.3: Output voltage waveform after zoomed in

Figure 5.4 shows the inductor current waveform after zoomed in. From the figure, it can be seen that the inductor current ripple is approximately 8.86 m – 8.85 m = 10 uA. Since the current regulation is supposed to be 1% of the maximum rated current, therefore, this value had met the requirement for the current regulation in the buck converter design.

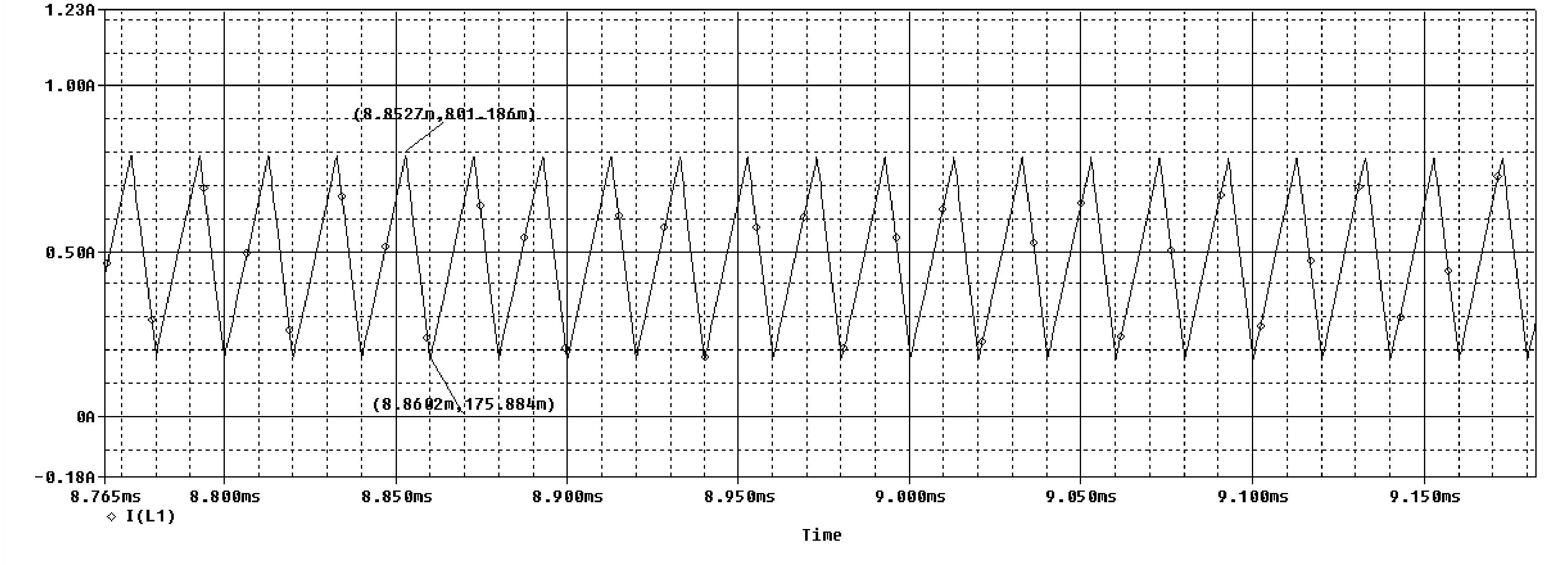


**Figure 5.4: Inductor current after zoomed in**

## 5.2 Hardware Results

Figure 5.5 shows the buck converter power stage circuit while Figure 5.6 shows the controller circuit and driver circuit constructed in one PCB and the Figre 5.7 shows the compensator circuit. The compensator circuit was not built on PCB so that it is easier to change the components' value during experiment to obtain the desired frequency response.

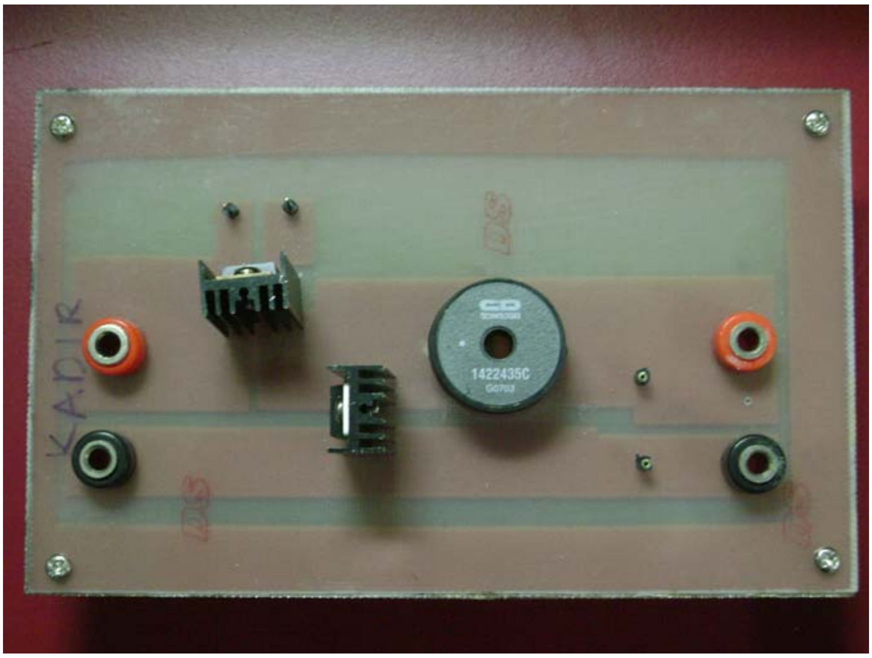


**Figure 5.5: Power stage circuit**

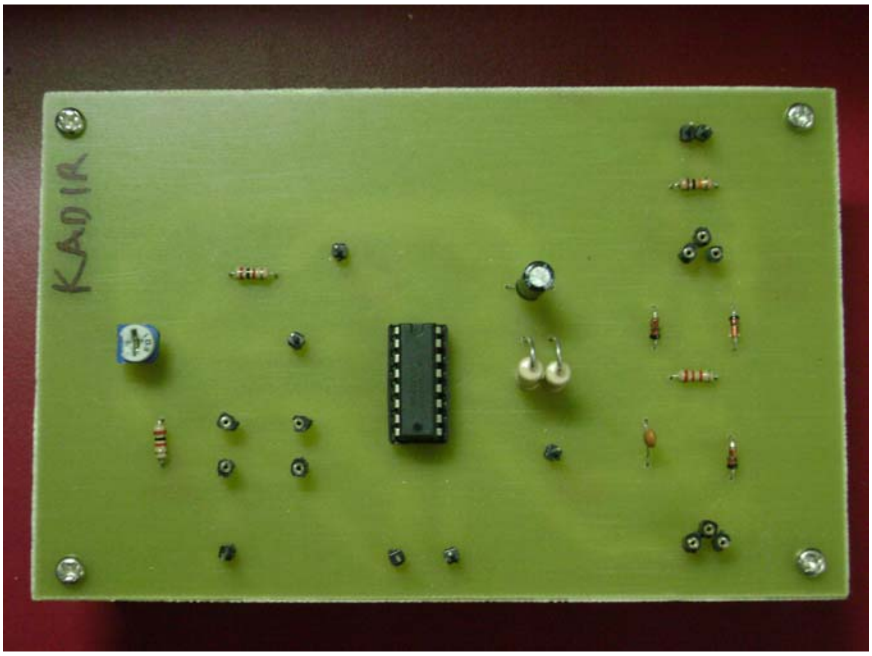


**Figure 5.6: Controller and driver circuit**

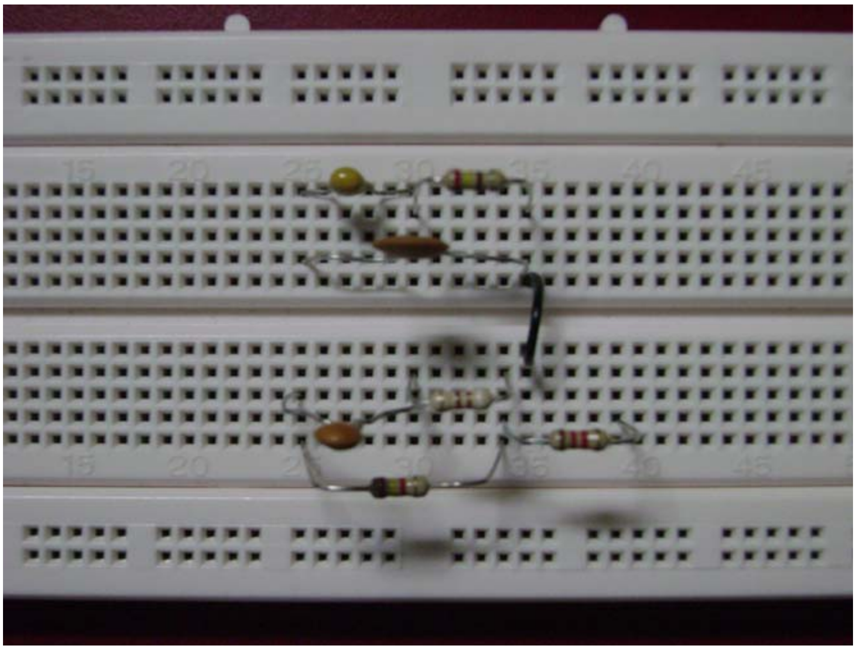


**Figure 5.7: Compensator circuit**

### 5.2.1 Open-loop Buck Converter

Figure 5.5 shows the output waveform from the controller and the driver circuit. The duty cycle of the pulse-width is approximately 50% or 0.5.

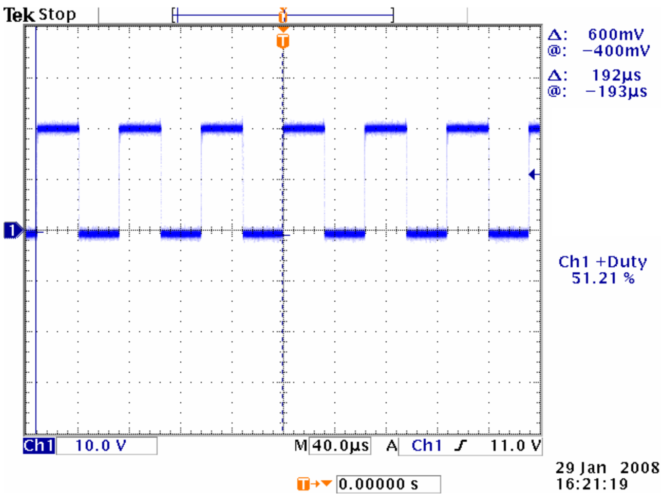


**Figure 5.8: Output waveform from controller and driver circuit**

Figure 5.6 shows the triangular waveform generated by the controller circuit. The maximum peak voltage of the triangular waveform is 3.6 V.

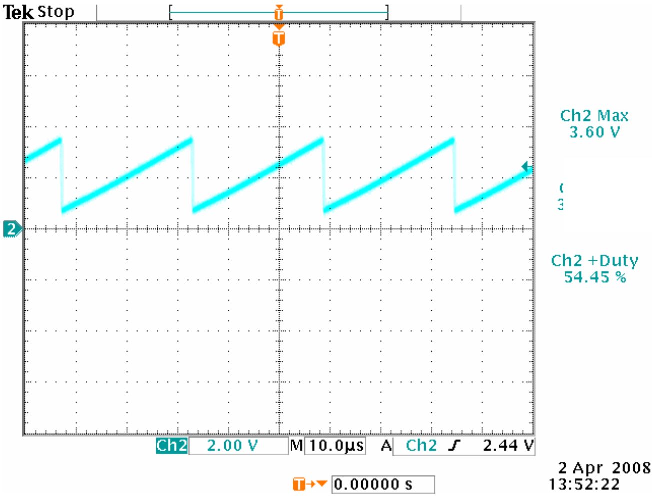


Figure 5.9: Triangular waveform generated by the controller circuit

Figure 5.7 shows the chopped input voltage waveform obtained from the diode. The waveform from the diode is the same with the output waveform from controller since the MOSFET was turned on and off by the pulse-width generated from the controller circuit. Thus, the pulse-width had chopped the input waveform and produces chopped input voltage waveform. Figure 5.8 shows the waveforms measured from the diode and output voltage waveform from the load.

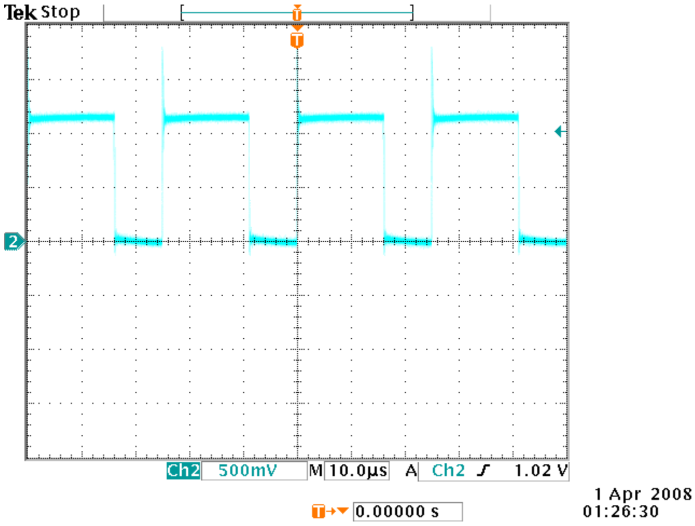


Figure 5.10: Input voltage waveform at the diode

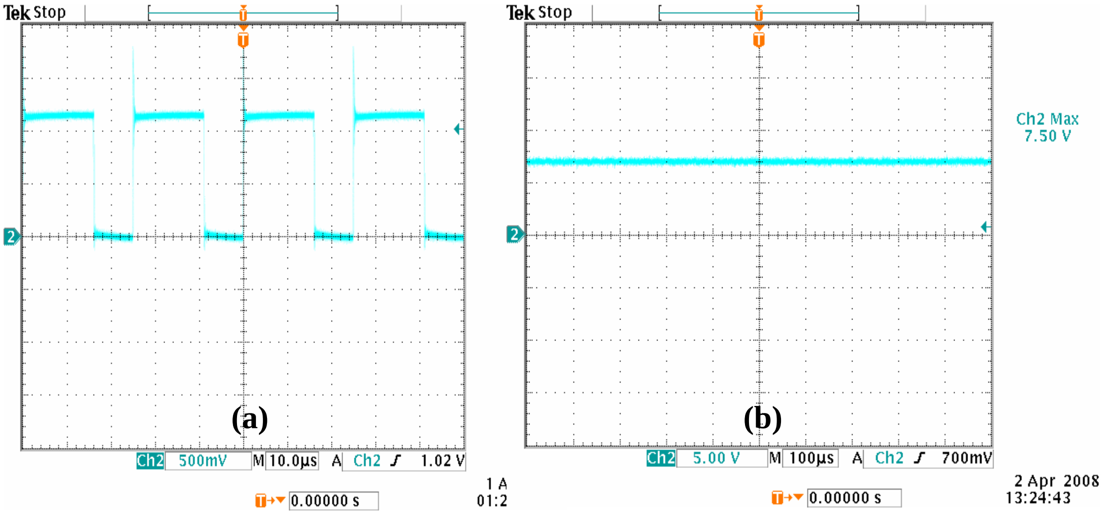


**Figure 5.11: (a) Chopped input voltage. (b) Output voltage waveform.**

### 5.2.2 Closed-loop Buck Converter

The following results show the regulation processed of the closed buck converter. In Figure 5.9 and Figure 5.10, the output voltage was regulated at 7.11 to 7.20 V. This value is closer to the design value which is 7.5 V. The output voltage is lower than the expected value is due to voltage drop in the circuit. In Figure 5.11, since the input voltage is out of the design range, the voltage dropped at much lower value (6.9 V). The changes in input voltage, causes the controller to vary the duty cycle to regulate the output voltage. The top waveform was taken from the diode and it is the chopped input voltage waveform while the bottom waveform was taken from the load at the power stage output which represents the output voltage actual response.

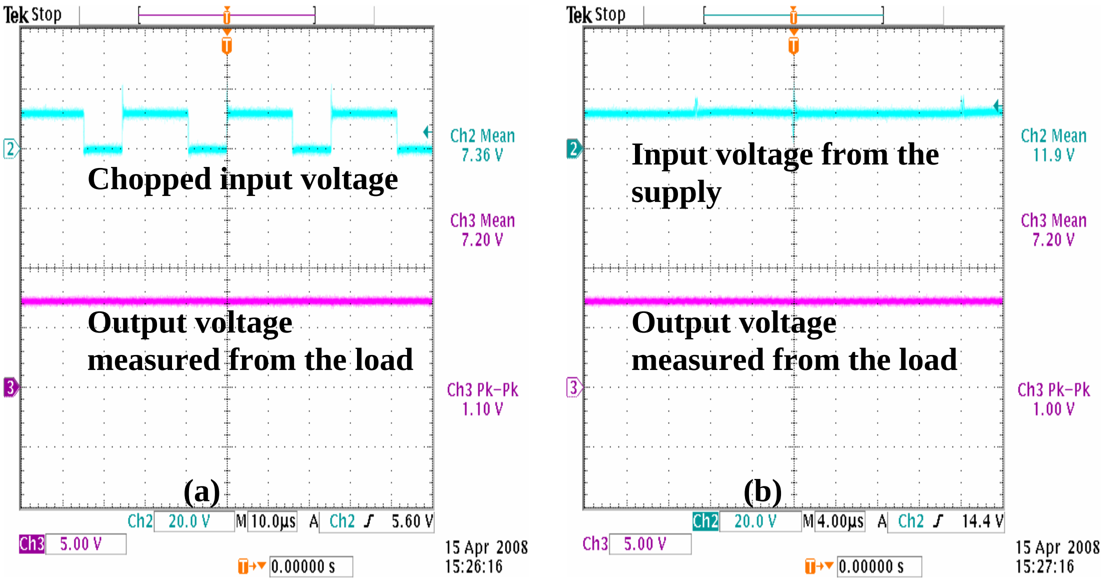


Figure 5.12: (a) Chopped input voltage and output voltage. (b) Input voltage (11.9 V) and output voltage.

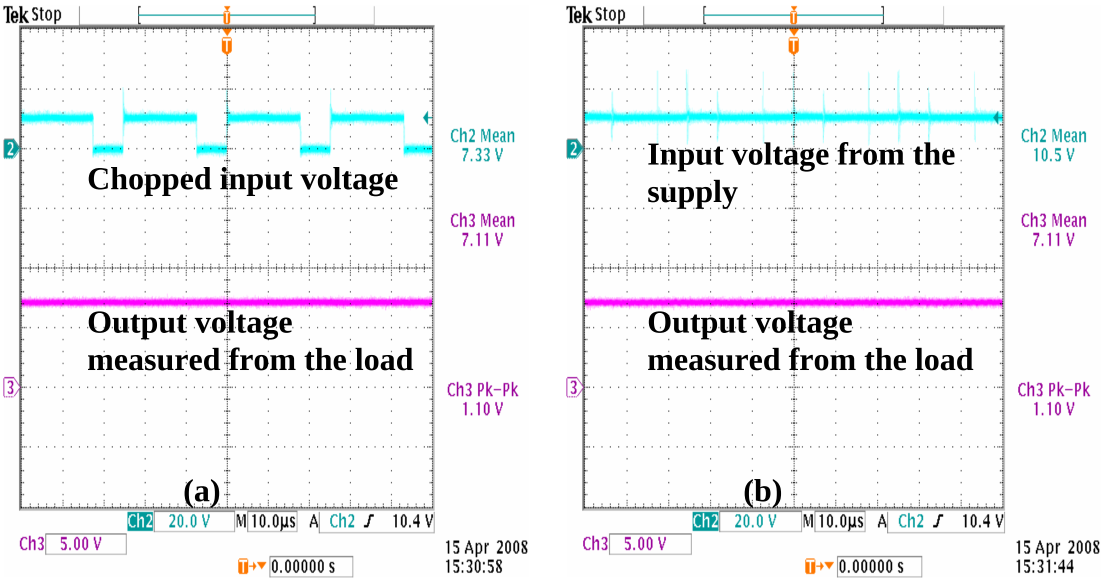


Figure 5.13: (a) Chopped input voltage and output voltage. (b) Input voltage (10.5 V) and output voltage.

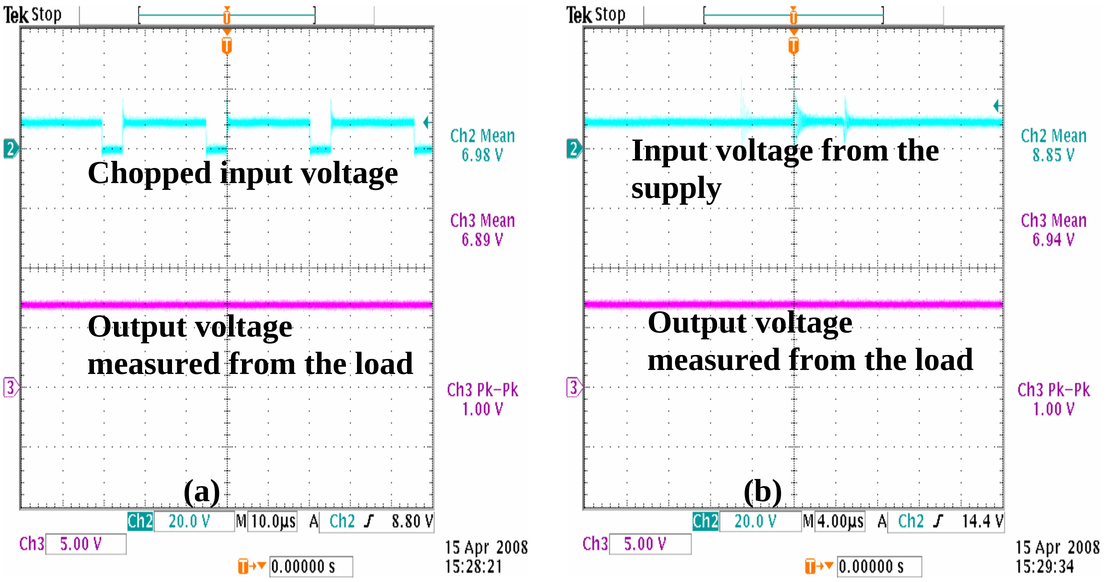


**Figure 5.14: (a) Chopped input voltage and output voltage. (b) Input voltage (8.85 V) and output voltage.**

# CHAPTER 6

# CONCLUSIONS AND SUGGESTIONS

## 6.0 Introduction

This final chapter concludes all the topics that have been discussed previously. In addition to the conclusion, some suggestions for future work on this project are described.

## 6.1 Suggestions For Future

Even though the proposed objectives has been met, there are still many improvement that could be done for this project. The project is far from completed since many improvement could be done to increase the reliability and accuracy of the converter.

Because the technology is still improving over the years, there are many types of configuration for buck converter control available in the market. For instance, there are synchronous buck converter, peak-current control buck converter and etc.

Thus, this project could be expanded by implementing peak-current mode control or synchronous buck configuration into the voltage-mode control buck converter for improvement in the controlling the output voltage. By improving the control method for the buck converter, the complexity of the design will arise, thus it will needs some study to be done in the future for such improvement.

Finally, even after such improvement, there will be more studies that could be done to improve the efficiency and reliability of the converter. The method of controlling the MOSFET by using pulse-width modulation generated by the microcontroller is one such study that could be done in the future.

## 6.2 Conclusions

As conclusion, this project had successfully achieved its main objectives which is to develop a voltage-mode control buck converter. The closed-loop circuit simplifies the tedious work of controlling the output by automatically adjusting the duty cycle to regulate the output voltage at a particular level.

Even though voltage-mode control sense the changes in output and input signal to regulate the voltage at specific level, it still can be expanded by adding other method such as peak-current control and synchronous buck configuration. However, this will add complexity to the design. Thus further research and studies are required for such expansion.

Voltage-mode control is chosen for this project since its design process is not very complex and not to mention, cheap. The controlling method is also easy to understand since it detects the voltage change through sense network and feed the signal back to the controller circuit for regulation process.

Last but not least, this project had also taught me many things in handling problems, providing and implementing solutions to solve them. Time management is also very important as last minute work can be very pressuring and tiring. Good time management is crucial since it ensures that this project can be finished on time with good quality of work.

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[8] Johari Kasim, Camallil Omar and Abd Hamid Ahmad; Modul Pengajaran Sistem Elektronik, edisi pertama; 2005; Universiti Teknologi Malaysia, Skudai, Johor, Malaysia.

[9] Michael (Chongming) Qiao, Parviz Parto et.al.; Stabilize the Buck Converter with Transconductance Amplifier; Application Note AN-1043; International Rectifier.

[10] Designing With the TL5001 PWM Controller; Application Report; Texas Instrument.

# APPENDICES

# APPENDIX A

## PLANNING FOR PSM 1

| NO | ACTIVITIES | WEEKS | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 1 | Final year project briefing | | ■ | | | | | | | | | | | | | |
| 2 | Selecting department | | | ■ | | | | | | | | | | | | |
| 3 | Selecting problem and title for FYP | | | ■ | ■ | | | | | | | | | | | |
| 4 | Searching for literature review and consultation with supervisor | | | | ■ | | | | | | | | | | | |
| 5 | Project proposal | | | | ■ | ■ | | | | | | | | | | |
| 6 | Submitting proposal | | | | ■ | ■ | ■ | ■ | | | | | | | | |
| 7 | Research and studies | | | | | | | ■ | | | | | | | | |
| 8 | Studying buck converter theory | | | | | | | ■ | | | | | | | | |
| 9 | Choosing design specification | | | | | | | ■ | ■ | | | | | | | |
| 10 | Designing buck converter components | | | | | | | ■ | ■ | | | | | | | |
| 11 | Simulation using PSpice | | | | | | | | | ■ | ■ | | | | | |
| 12 | Simulation of power stage using PSpice | | | | | | | | | ■ | ■ | | | | | |
| 13 | Consultation with supervisor | | | | | | | | | ■ | ■ | | | | | |
| 14 | First seminar | | | | | | | | | | ■ | ■ | | | | |
| 15 | Studying closed-loop design | | | | | | | | | | | | ■ | ■ | | |
| 16 | Designing controller circuit | | | | | | | | | | | | | ■ | ■ | |
| 17 | Simulation of the control circuit | | | | | | | | | | | | | ■ | ■ | |
| 18 | Constructs and simulates the new converter circuit by using PSpice | | | | | | | | | | | | | ■ | ■ | |
| 19 | Consultation with supervisor | | | | | | | | | | | | | ■ | ■ | |
| 20 | Preparing the FYP 1 report | | | | | | | | | | | | | ■ | ■ | ■ |

# APPENDIX B

**PLANNING FOR PSM 2**

| NO | ACTIVITIES | WEEKS | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |
| **1** | **Design PID controller** | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | | | | |
| **2** | **Consultation with supervisor** | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | | | | |
| **3** | **Ordering components from Farnell** | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | | | | |
| **4** | **Bode plot simulation for complete buck converter** | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | | | | |
| **5** | **Build PCB circuits** | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | | | | |
| **6** | **Submitting form PSM 2-0** | | | ■ | ■ | | | | | | | | | | | | | | |
| **7** | **Submitting form PSM 2-1** | | | | | | | | | | ■ | ■ | ■ | | | | | | |
| **8** | **Testing and analyzing the hardware** | | | | | | | ■ | ■ | ■ | ■ | ■ | ■ | ■ | | | | | |
| **9** | **Preparation for final seminar and final presentation** | | | | | | | ■ | ■ | ■ | ■ | ■ | ■ | ■ | | | | | |
| **10** | **Preparing the thesis draft** | | | | | | | ■ | ■ | ■ | ■ | ■ | ■ | ■ | | | | | |
| **11** | **Final seminar and demonstration** | | | | | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | | | | |
| **12** | **Submit the thesis draft** | | | | | | | | | | | | | | | ■ | | | |
| **13** | **Thesis writing work** | | | | | | | | | | | | | | | ■ | ■ | ■ | |
| **14** | **Submitting completed thesis with hardcover** | | | | | | | | | | | | | | | | | | ■ |

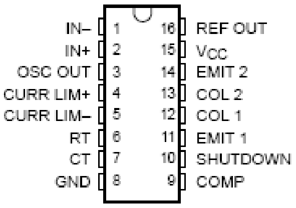
# APPENDIX C

# SG2524, SG3524
# REGULATING PULSE-WIDTH MODULATORS

SLVS077D – APRIL 1977 – REVISED FEBRUARY 2003

- **Complete Pulse-Width Modulation (PWM) Power-Control Circuitry**
- **Uncommitted Outputs for Single-Ended or Push-Pull Applications**
- **Low Standby Current . . . 8 mA Typ**
- **Interchangeable With Industry Standard SG2524 and SG3524**

**SG2524 . . . D OR N PACKAGE**
**SG3524 . . . D, N, OR NS PACKAGE**
**(TOP VIEW)**



## description/ordering information

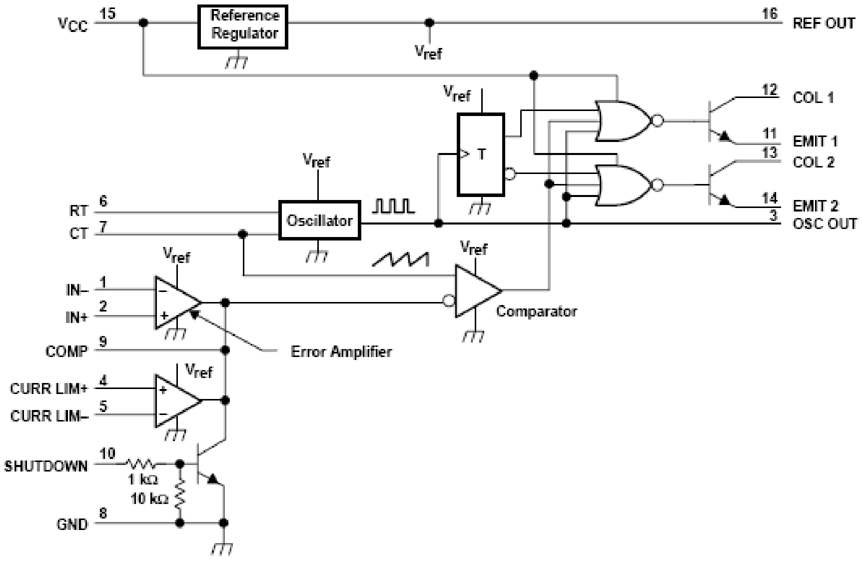
The SG2524 and SG3524 incorporate all the functions required in the construction of a regulating power supply, inverter, or switching regulator on a single chip. They also can be used as the control element for high-power-output applications. The SG2524 and SG3524 were designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers, and polarity-converter applications employing fixed-frequency, pulse-width modulation (PWM) techniques. The complementary output allows either single-ended or push-pull application. Each device includes an on-chip regulator, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted pass transistors, a high-gain comparator, and current-limiting and shutdown circuitry.

ORDERING INFORMATION

| $T_A$ | INPUT REGULATION MAX (mV) | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|---|
| 0°C to 70°C | 30 | PDIP (N) | Tube of 25 | SG3524N | SG3524N |
| | | SOIC (D) | Tube of 40 | SG3524D | SG3524 |
| | | | Reel of 2500 | SG3524DR | |
| | | SOP (NS) | Reel of 2000 | SG3524NSR | SG3524 |
| –25°C to 85°C | 20 | PDIP (N) | Tube of 25 | SG2524N | SG2524N |
| | | SOIC (D) | Tube of 40 | SG2524D | SG2524 |
| | | | Reel of 2500 | SG2524DR | |

† Package drawings, standard packing quantities, thermal data, symboliztion, and PCB design guidelines are available at www.ti.com/sc/package.

### functional block diagram



NOTE A: Resistor values shown are nominal.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | | |
|---|---|---|
| Supply voltage, $V_{CC}$ (see Notes 1 and 2) | | 40 V |
| Collector output current, $I_{CC}$ | | 100 mA |
| Reference output current, $I_{O(ref)}$ | | 50 mA |
| Current through CT terminal | | –5 mA |
| Operating virtual junction temperature, $T_J$ | | 150°C |
| Package thermal impedance, $\theta_{JA}$ (see Notes 3 and 4): | D package | 73°C/W |
| | N package | 67°C/W |
| | NS package | 64°C/W |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 260°C |
| Storage temperature range, $T_{stg}$ | | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values are with respect to network ground terminal.
2. The reference regulator may be bypassed for operation from a fixed 5-V supply by connecting the $V_{CC}$ and reference output (REF OUT) pin both to the supply voltage. In this configuration, the maximum supply voltage is 6 V.
3. Maximum power dissipation is a function of $T_{J(max)}$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operation at the absolute maximum $T_J$ of 150°C can impact reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 8 | 40 | V |
| | Reference output current | | 0 | 50 | mA |
| | Current through CT terminal | | –0.03 | –2 | mA |
| $R_T$ | Timing resistor | | 1.8 | 100 | kΩ |
| $C_T$ | Timing capacitor | | 0.001 | 0.1 | µF |
| $T_A$ | Operating free-air temperature | SG2524 | –25 | 85 | °C |
| | | SG3524 | 0 | 70 | |

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 20 V, f = 20 kHz (unless otherwise noted)

### reference section

| PARAMETER | TEST CONDITIONS† | SG2524 | | | SG3524 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| Output voltage | | 4.8 | 5 | 5.2 | 4.6 | 5 | 5.4 | V |
| Input regulation | $V_{CC}$ = 8 V to 40 V | | 10 | 20 | | 10 | 30 | mV |
| Ripple rejection | f = 120 Hz | | 66 | | | 66 | | dB |
| Output regulation | $I_O$ = 0 mA to 20 mA | | 20 | 50 | | 20 | 50 | mV |
| Output voltage change with temperature | $T_A$ = MIN to MAX | | 0.3% | 1% | | 0.3% | 1% | |
| Short-circuit output current§ | $V_{ref}$ = 0 | | 100 | | | 100 | | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at $T_A$ = 25°C
§ Standard deviation is a measure of the statistical distribution about the mean, as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

### oscillator section

| | PARAMETER | TEST CONDITIONS† | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{osc}$ | Oscillator frequency | $C_T$ = 0.001 µF, $R_T$ = 2 kΩ | | 450 | | kHz |
| | Standard deviation of frequency§ | All values of voltage, temperature, resistance, and capacitance constant | | 5% | | |
| $\Delta f_{osc}$ | Frequency change with voltage | $V_{CC}$ = 8 V to 40 V, $T_A$ = 25°C | | | 1% | |
| | Frequency change with temperature | $T_A$ = MIN to MAX | | | 2% | |
| | Output amplitude at OSC OUT | $T_A$ = 25°C | | 3.5 | | V |
| $t_w$ | Output pulse duration (width) at OSC OUT | $C_T$ = 0.01 µF, $T_A$ = 25°C | | 0.5 | | µs |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at $T_A$ = 25°C
§ Standard deviation is a measure of the statistical distribution about the mean, as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N - 1}}$$

### error amplifier section

| PARAMETER | | TEST CONDITIONS† | SG2524 | | | SG3524 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IO}$ | Input offset voltage | $V_{IC}$ = 2.5 V | | 0.5 | 5 | | 2 | 10 | mV |
| $I_{IB}$ | Input bias current | $V_{IC}$ = 2.5 V | | 2 | 10 | | 2 | 10 | μA |
| | Open-loop voltage amplification | | 72 | 80 | | 60 | 80 | | dB |
| $V_{ICR}$ | Common-mode input voltage range | $T_A$ = 25°C | 1.8 to 3.4 | | | 1.8 to 3.4 | | | V |
| CMMR | Common-mode rejection ratio | | | 70 | | | 70 | | dB |
| $B_1$ | Unity-gain bandwidth | | | 3 | | | 3 | | MHz |
| | Output swing | $T_A$ = 25°C | 0.5 | | 3.8 | 0.5 | | 3.8 | V |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at $T_A$ = 25°C

### output section

| PARAMETER | | TEST CONDITIONS† | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(BR)CE}$ | Collector-emitter breakdown voltage | | 40 | | | V |
| | Collector off-state current | $V_{CE}$ = 40 V | | 0.01 | 50 | μA |
| $V_{sat}$ | Collector-emitter saturation voltage | $I_C$ = 50 mA | | 1 | 2 | V |
| $V_O$ | Emitter output voltage | $V_C$ = 20 V, $I_E$ = –250 μA | 17 | 18 | | V |
| $t_r$ | Turn-off voltage rise time | $R_C$ = 2 kΩ | | 0.2 | | μs |
| $t_f$ | Turn-on voltage fall time | $R_C$ = 2 kΩ | | 0.1 | | μs |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at $T_A$ = 25°C.

### comparator section

| PARAMETER | | TEST CONDITIONS† | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Maximum duty cycle, each output | | 45% | | | |
| $V_{IT}$ | Input threshold voltage at COMP | Zero duty cycle | | 1 | | V |
| | | Maximum duty cycle | | 3.5 | | |
| $I_{IB}$ | Input bias current | | | –1 | | μA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for temperature coefficients, are at $T_A$ = 25°C.

### current limiting section

| PARAMETER | | TEST CONDITIONS† | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_I$ | Input voltage range (either input) | | –1 to1 | | | V |
| $V_{(SENSE)}$ | Sense voltage at $T_A$ = 25°C | $V_{(IN+)} - V_{(IN–)} \geq 50$ mV, $V_{(COMP)}$ = 2 V | 175 | 200 | 225 | mV |
| | Temperature coefficient of sense voltage | | | 0.2 | | mV/°C |

‡ All typical values, except for temperature coefficients, are at $T_A$ = 25°C.

### total device

| PARAMETER | | TEST CONDITIONS | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{st}$ | Standby current | $V_{CC}$ = 40 V, IN–, CURR LIM+, $C_T$, GND, COMP, EMIT 1, EMIT 2 grounded, IN+ at 2 V, All other inputs and outputs open | | 8 | 10 | mA |

‡ All typical values, except for temperature coefficients, are at $T_A$ = 25°C.

## PARAMETER MEASUREMENT INFORMATION

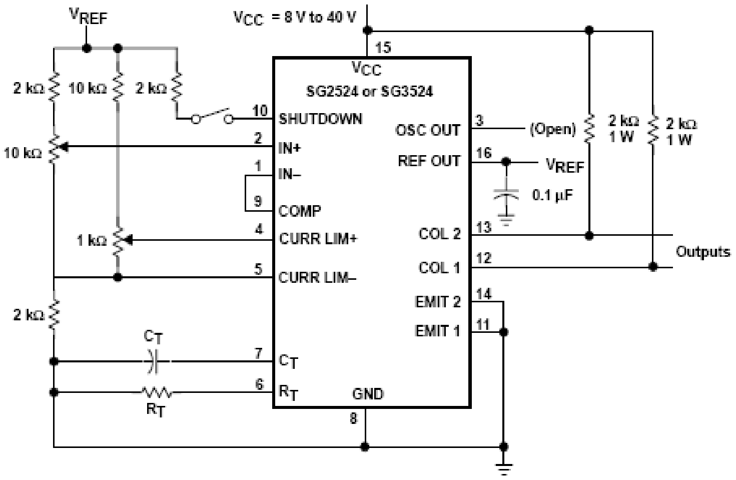
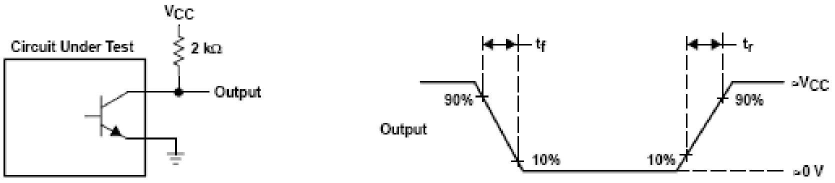


Figure 1. General Test Circuit



TEST CIRCUIT

VOLTAGE WAVEFORMS

Figure 2. Switching Times

## TYPICAL CHARACTERISTICS

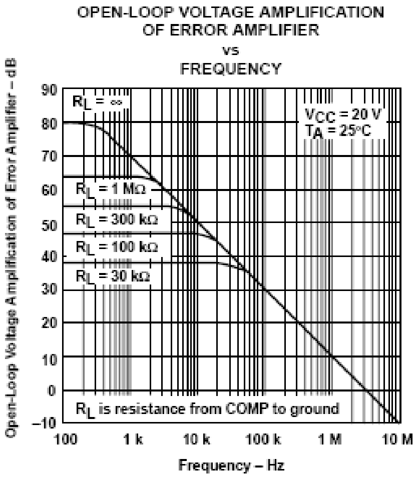


Figure 3

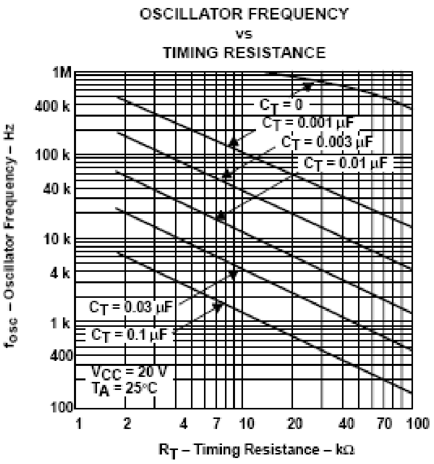


Figure 4

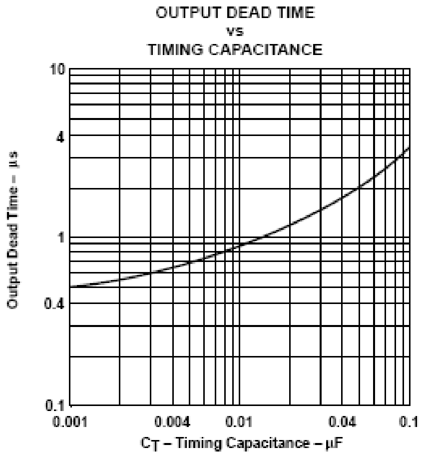


Figure 5

## PRINCIPLES OF OPERATION[†]

The SG2524 is a fixed-frequency pulse-width-modulation (PWM) voltage-regulator control circuit. The regulator operates at a fixed frequency that is programmed by one timing resistor, $R_T$, and one timing capacitor, $C_T$. $R_T$ establishes a constant charging current for $C_T$. This results in a linear voltage ramp at $C_T$, which is fed to the comparator, providing linear control of the output pulse duration (width) by the error amplifier. The SG2524 contains an onboard 5-V regulator that serves as a reference, as well as supplying the SG2524 internal regulator control circuitry. The internal reference voltage is divided externally by a resistor ladder network to provide a reference within the common-mode range of the error amplifier as shown in Figure 6, or an external reference can be used. The output is sensed by a second resistor divider network and the error signal is amplified. This voltage is then compared to the linear voltage ramp at $C_T$. The resulting modulated pulse out of the high-gain comparator then is steered to the appropriate output pass transistor (Q1 or Q2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to ensure both outputs are never on simultaneously during the transition times. The duration of the blanking pulse is controlled by the value of $C_T$. The outputs may be applied in a push-pull configuration in which their frequency is one-half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current-limiting and shut-down circuitry and can be overridden by signals from either of these inputs. This common point is pinned out externally via the COMP pin, which can be employed to either control the gain of the error amplifier or to compensate it. In addition, the COMP pin can be used to provide additional control to the regulator.

## APPLICATION INFORMATION[†]

### oscillator

The oscillator controls the frequency of the SG2524 and is programmed by $R_T$ and $C_T$ as shown in Figure 4.

$$f \approx \frac{1.30}{R_T\, C_T}$$

where: $R_T$ is in kΩ
$C_T$ is in μF
f is in kHz

Practical values of $C_T$ fall between 0.001 μF and 0.1 μF. Practical values of $R_T$ fall between 1.8 kΩ and 100 kΩ. This results in a frequency range typically from 130 Hz to 722 kHz.

### blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse duration is controlled by the value of $C_T$ as shown in Figure 5. If small values of $C_T$ are required, the oscillator output pulse duration can be maintained by applying a shunt capacitance from OSC OUT to ground.

### synchronous operation

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kΩ. In this configuration, $R_TC_T$ must be selected for a clock period slightly greater than that of the external clock.

---

[†] Throughout these discussions, references to the SG2524 apply also to the SG3524.

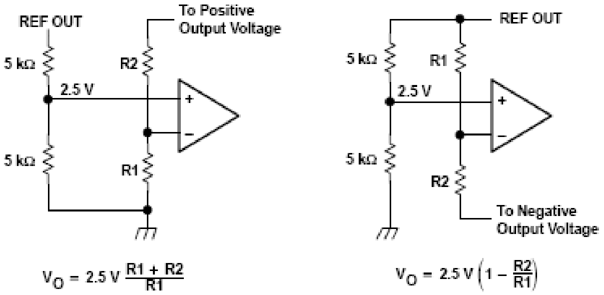
## APPLICATION INFORMATION[†]

### synchronous operation (continued)

If two or more SG2524 regulators are operated synchronously, all oscillator output terminals must be tied together. The oscillator programmed for the minimum clock period is the master from which all the other SG2524s operate. In this application, the $C_TR_T$ values of the slaved regulators must be set for a period approximately 10% longer than that of the master regulator. In addition, $C_T$ (master) = 2 $C_T$ (slave) to ensure that the master output pulse, which occurs first, has a longer pulse duration and, subsequently, resets the slave regulators.

### voltage reference

The 5-V internal reference can be employed by use of an external resistor divider network to establish a reference common-mode voltage range (1.8 V to 3.4 V) within the error amplifiers (see Figure 6), or an external reference can be applied directly to the error amplifier. For operation from a fixed 5-V supply, the internal reference can be bypassed by applying the input voltage to both the $V_{CC}$ and $V_{REF}$ terminals. In this configuration, however, the input voltage is limited to a maximum of 6 V.



$$V_O = 2.5\ \text{V}\ \frac{R1 + R2}{R1}$$

$$V_O = 2.5\ \text{V}\left(1 - \frac{R2}{R1}\right)$$

Figure 6. Error-Amplifier Bias Circuits

### error amplifier

The error amplifier is a differential-input transconductance amplifier. The output is available for dc gain control or ac phase compensation. The compensation node (COMP) is a high-impedance node ($R_L$ = 5 MΩ). The gain of the amplifier is $A_V = (0.002\ \Omega^{-1})R_L$ and easily can be reduced from a nominal 10,000 by an external shunt resistance from COMP to ground. Refer to Figure 3 for data.

### compensation

COMP, as previously discussed, is made available for compensation. Since most output filters introduce one or more additional poles at frequencies below 200 Hz, which is the pole of the uncompensated amplifier, introduction of a zero to cancel one of the output filter poles is desirable. This can be accomplished best with a series RC circuit from COMP to ground in the range of 50 kΩ and 0.001 µF. Other frequencies can be canceled by use of the formula f ≈ 1/RC.

---

[†] Throughout these discussions, references to the SG2524 apply also to the SG3524.

## APPLICATION INFORMATION†

### shutdown circuitry

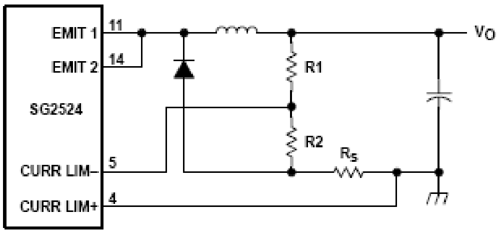
COMP also can be employed to introduce external control of the SG2524. Any circuit that can sink 200 μA can pull the compensation terminal to ground and, thus, disable the SG2524.

In addition to constant-current limiting, CURR LIM+ and CURR LIM– also can be used in transformer-coupled circuits to sense primary current and shorten an output pulse should transformer saturation occur. CURR LIM– also can be grounded to convert CURR LIM+ into an additional shutdown terminal.

### current limiting

A current-limiting sense amplifier is provided in the SG2524. The current-limiting sense amplifier exhibits a threshold of 200 mV ±25 mV and must be applied in the ground line since the voltage range of the inputs is limited to 1 V to –1 V. Caution should be taken to ensure the –1-V limit is not exceeded by either input, otherwise, damage to the device may result.

Foldback current limiting can be provided with the network shown in Figure 7. The current-limit schematic is shown in Figure 8.



$$I_{O(max)} = \frac{1}{R_S}\left(200\ \text{mV} + \frac{V_O\,R2}{R1 + R2}\right)$$

$$I_{OS} = \frac{200\ \text{mV}}{R_S}$$

**Figure 7. Foldback Current Limiting for Shorted Output Conditions**

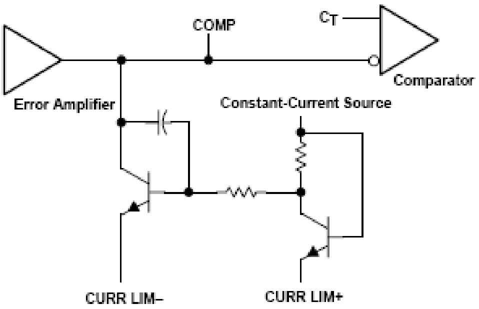


**Figure 8. Current-Limit Schematic**

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† Throughout these discussions, references to the SG2524 apply also to the SG3524.

## APPLICATION INFORMATION†

### output circuitry

The SG2524 contains two identical npn transistors, the collectors and emitters of which are uncommitted. Each transistor has antisaturation circuitry that limits the current through that transistor to a maximum of 100 mA for fast response.

### general

There are a wide variety of output configurations possible when considering the application of the SG2524 as a voltage-regulator control circuit. They can be segregated into three basic categories:

- Capacitor-diode-coupled voltage multipliers
- Inductor-capacitor-implemented single-ended circuits
- Transformer-coupled circuits

Examples of these categories are shown in Figures 9, 10, and 11, respectively. Detailed diagrams of specific applications are shown in Figures 12–15.

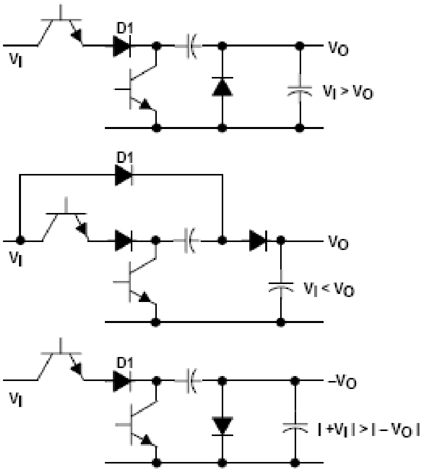

Figure 9. Capacitor-Diode-Coupled Voltage-Multiplier Output Stages

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† Throughout these discussions, references to the SG2524 apply also to the SG3524.

## APPLICATION INFORMATION†

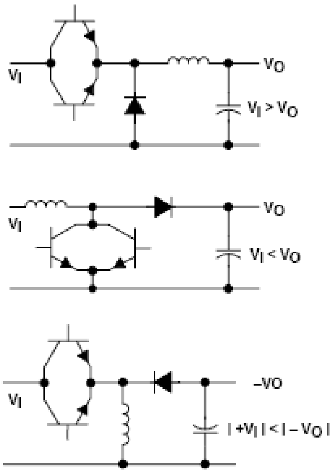
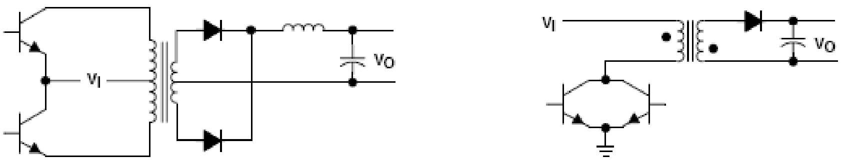


Figure 10. Single-Ended Inductor Circuit



Push-Pull

Flyback

Figure 11. Transformer-Coupled Outputs

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† Throughout these discussions, references to the SG2524 apply also to the SG3524.

## APPLICATION INFORMATION†

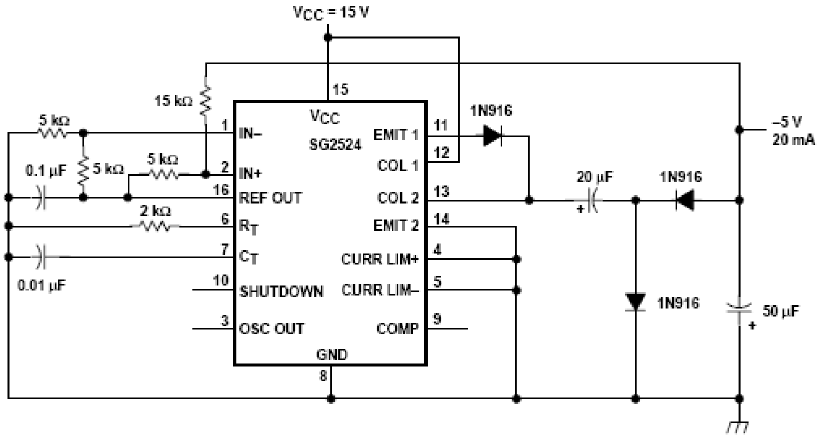

Figure 12. Capacitor-Diode Output Circuit

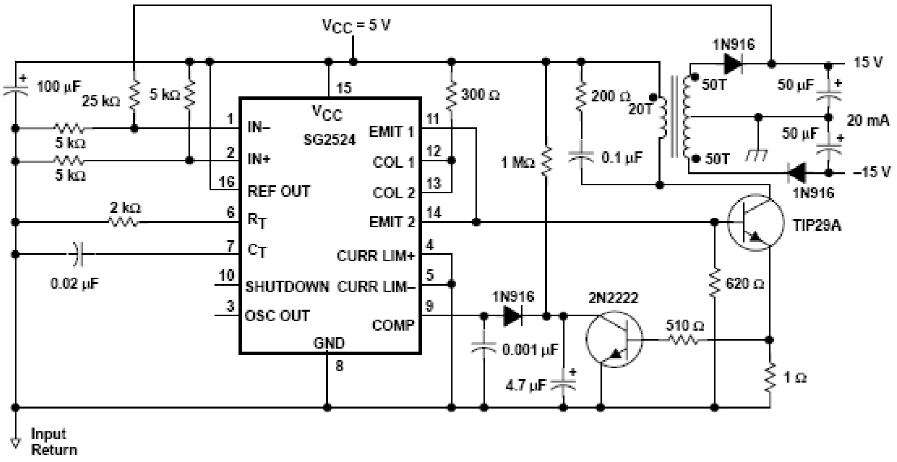

Figure 13. Flyback Converter Circuit

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†Throughout these discussions, references to the SG2524 apply also to the SG3524.

## APPLICATION INFORMATION†

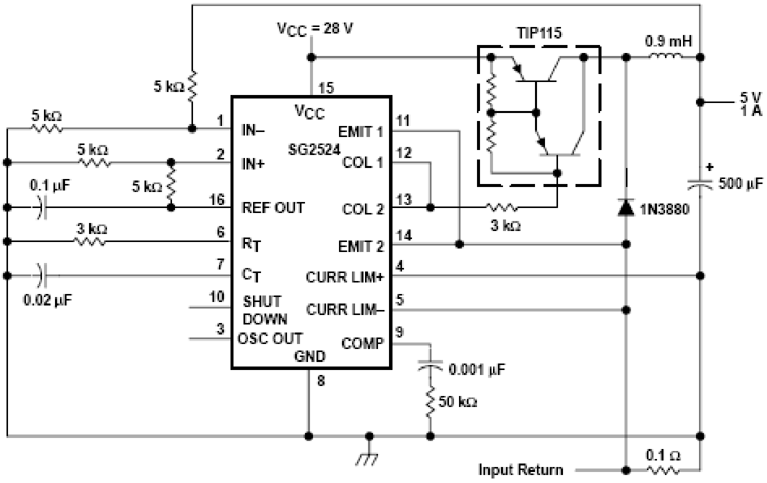

Figure 14. Single-Ended LC Circuit

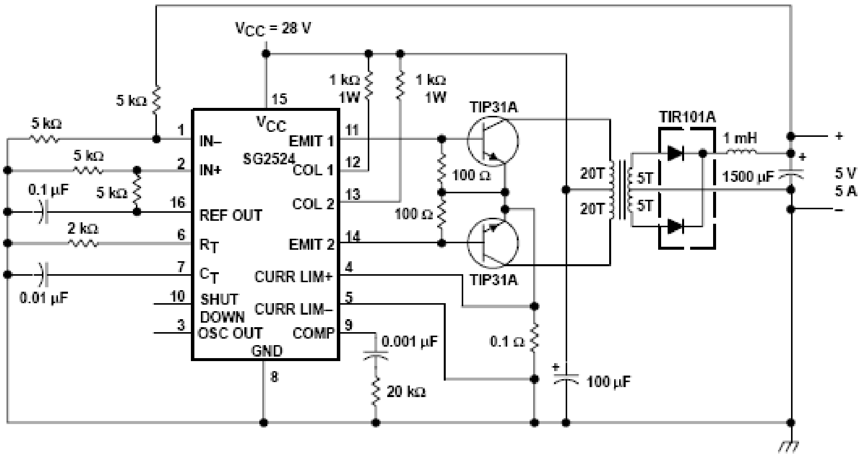

Figure 15. Push-Pull Transformer-Coupled Circuit

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† Throughout these discussions, references to the SG2524 apply also to the SG3524.

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| SG2524D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SG2524DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SG2524DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SG2524DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SG2524J | OBSOLETE | CDIP | J | 16 |  | TBD | Call TI | Call TI |
| SG2524N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SG2524NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SG3524D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SG3524DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SG3524DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SG3524DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SG3524J | OBSOLETE | CDIP | J | 16 |  | TBD | Call TI | Call TI |
| SG3524N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SG3524NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SG3524NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SG3524NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. – The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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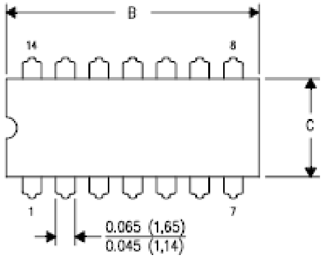
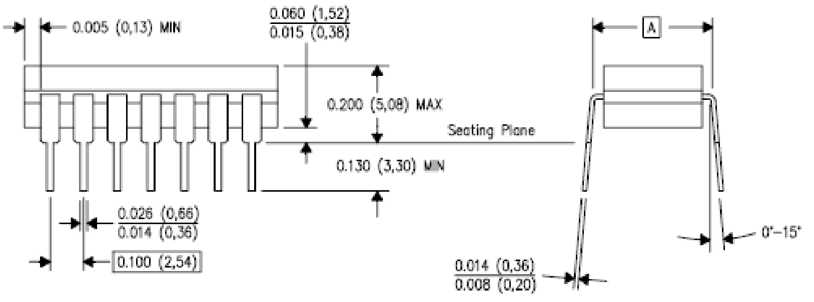
## J (R–GDIP–T**)　　CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



| PINS ** / DIM | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX | 0.785<br>(19,94) | .840<br>(21,34) | 0.960<br>(24,38) | 1.060<br>(26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300<br>(7,62) | 0.300<br>(7,62) | 0.310<br>(7,87) | 0.300<br>(7,62) |
| C MIN | 0.245<br>(6,22) | 0.245<br>(6,22) | 0.220<br>(5,59) | 0.245<br>(6,22) |

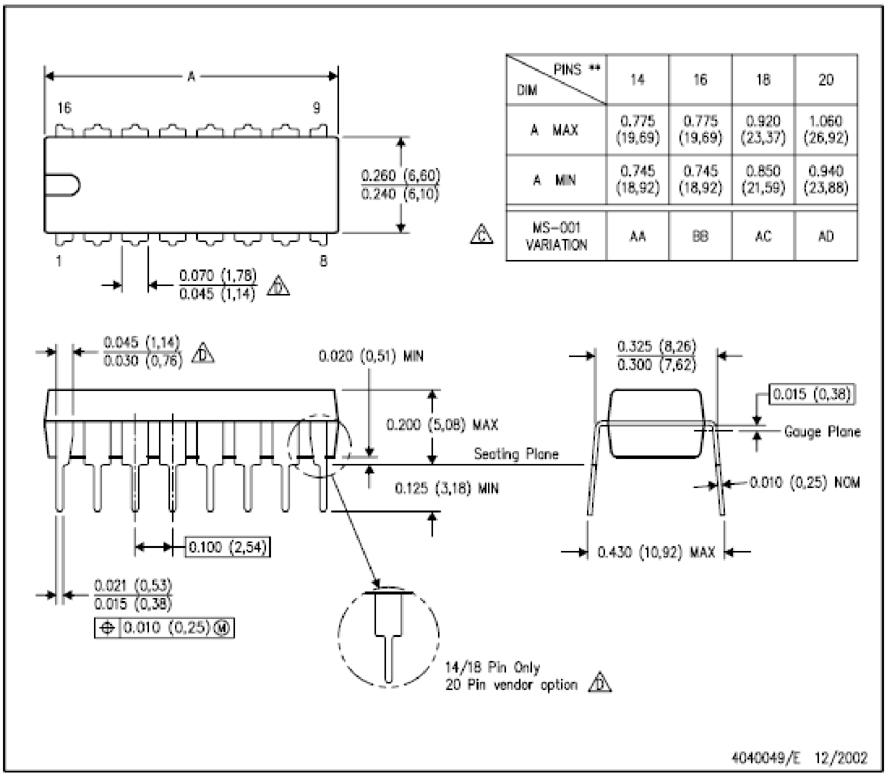


4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

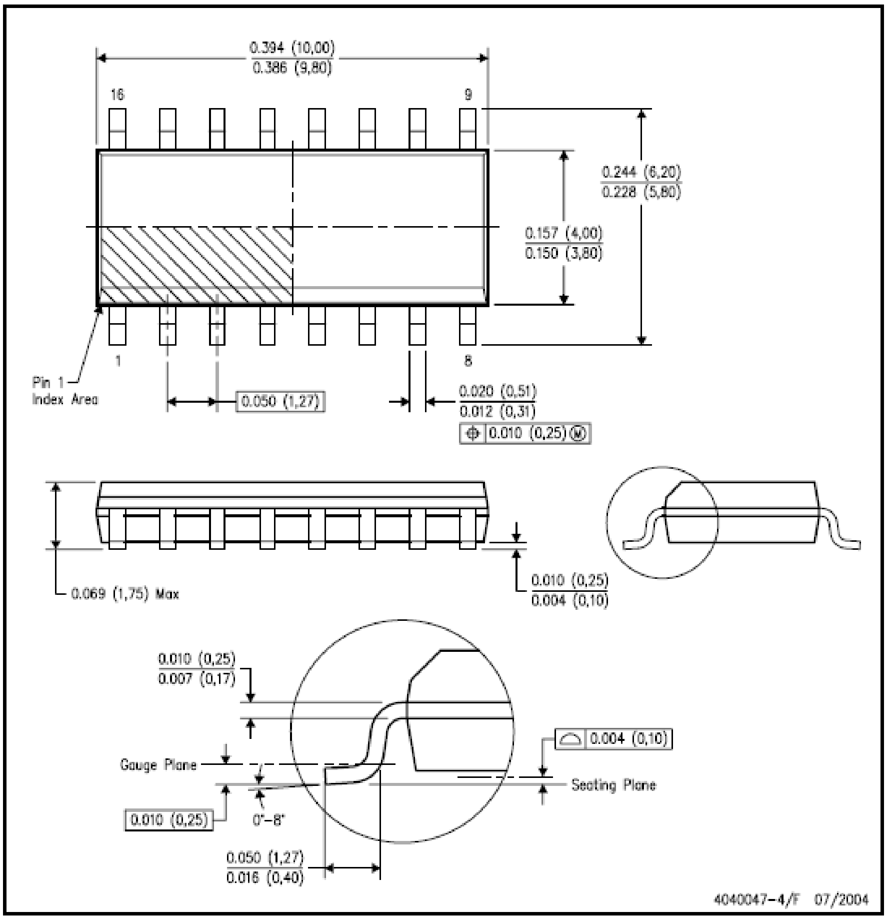
16 PINS SHOWN



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS–001 VARIATION | AA | BB | AC | AD |

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE

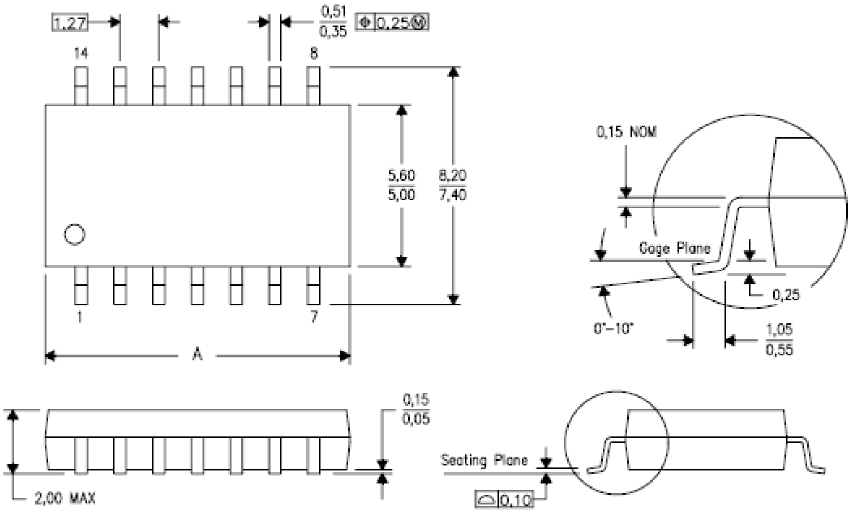


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–012 variation AC.

# MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



| PINS **<br>DIM | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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# APPENDIX D

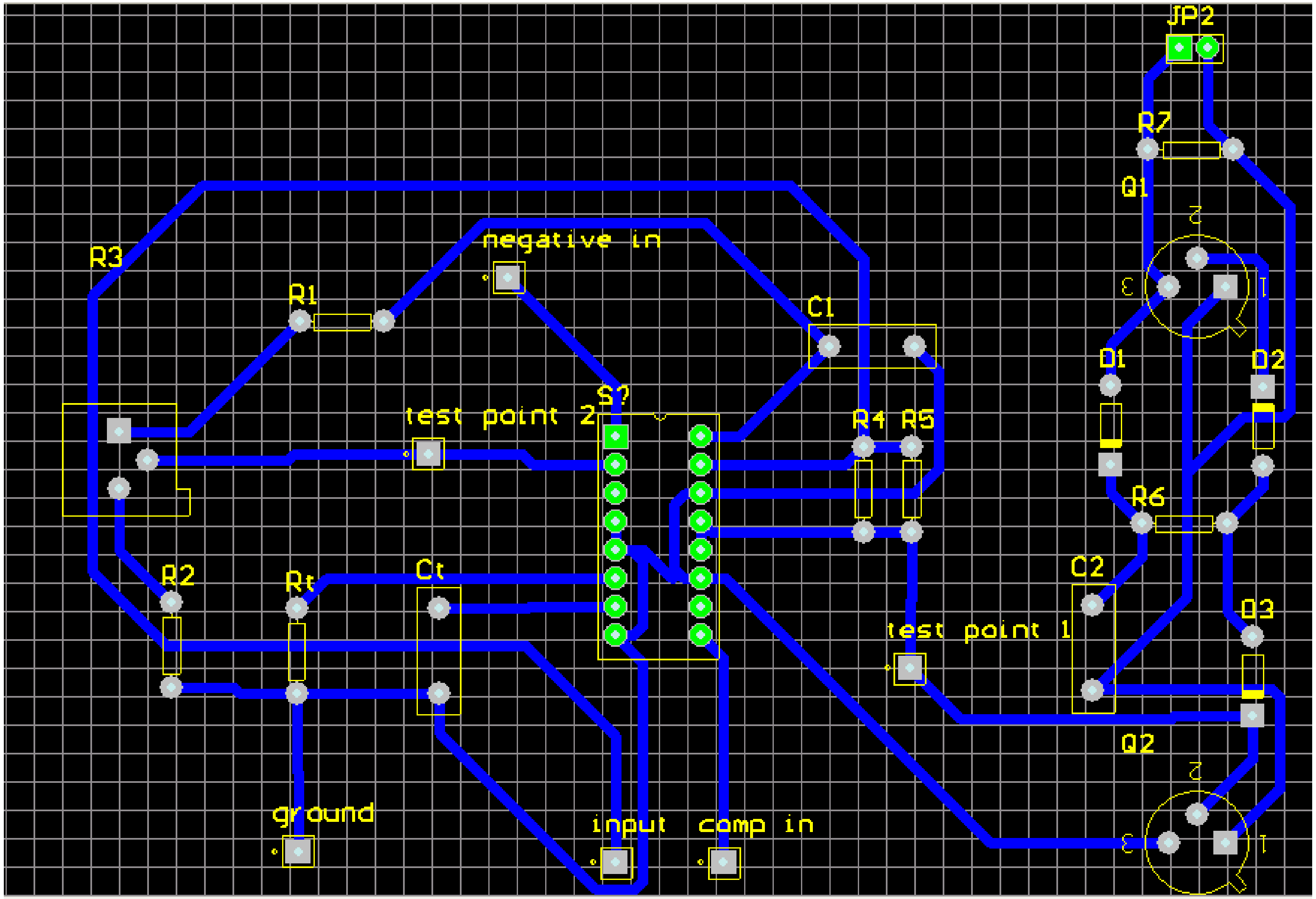

Figure 6: Controller’s PCB circuit

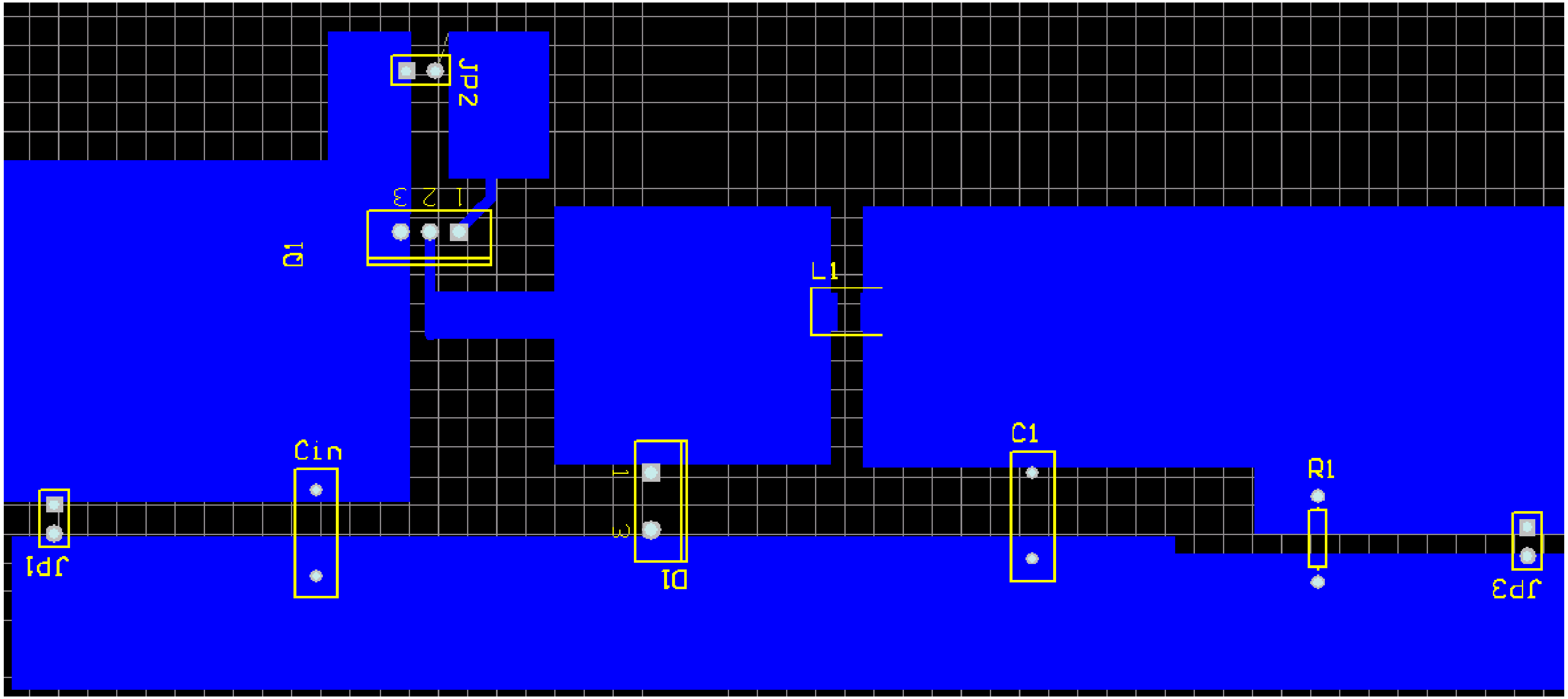

Figure 7: Buck converter power stage’s PCB circuit